AN ASSESSMENT OF COMPLEMENTARY SILICON-GERMANIUM BICMOS TECHNOLOGIES FOR EXTREME ENVIRONMENT APPLICATIONS

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AN ASSESSMENT OF COMPLEMENTARY SILICON-GERMANIUM BICMOS TECHNOLOGIES FOR EXTREME ENVIRONMENT APPLICATIONS

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SUMMARY

The objective of the proposed research is to assess the potential of complementary Silicon-Germanium (SiGe) BiCMOS technologies for extreme environment applications, specifically, radiation-intense environments. We have investigated the single-event response of analog, RF, and digital circuits designed using only *npn* or only *pnp* SiGe heterojunction bipolar transistors (HBTs). This document is organized as follows.

Chapter 1 provides an introduction to SiGe technology and radiation effects on SiGe heterojunction bipolar transistors (HBTs).

Chapter 2 focuses on analog circuits, and presents pulsed-laser results for comparator pre-amplifiers designed using only *npn* or only *pnp* devices. This work was published in *IEEE Transactions on Nuclear Science* [3]:

> A. Ildefonso, N. E. Lourenco, Z. E. Fleetwood, M. T. Wachter, G. N. Tzintzarov, A. S. Cardoso, N. J. H. Roche, A. Khachatrian, D. McMorrow, S. P. Buchner, J. H. Warner, P. Paki, M. Kaynak, B. Tillack, and J. D. Cressler, Single-Event Transient Response of Comparator Pre-Amplifiers in a Complementary SiGe Technology, *IEEE Trans. Nucl. Sci.*, vol. 64, pp. 8996, Jan. 2017.

Chapter 3 presents, through the use of mixed-mode TCAD simulations, the trade-offs between RF circuit performance and single-event transient robustness of two low-noise amplifiers designed using only *npn* or only *pnp* devices.

Chapter 4 shows the first heavy-ion study on a bulk, complementary SiGe platform by using high-speed digital structures using only *npn* devices and only *pnp* devices. This work as been accepted for presentation at the 2017 Nuclear and Space Radiation

Effects Conference (NSREC) and is slated for submission to the IEEE Transactions on Nuclear Science.

Chapter 5 includes some concluding remarks, summarizes the author's contributions and presents some ideas for possible future work.

CHAPTER I

INTRODUCTION

The global electronics market is dominated by silicon (Si) technology. The demand for highly-integrated, high-speed digital circuits has pushed the advancement of Si CMOS development, resulting in great progress of fabrication techniques for highly scaled devices and circuits. As circuits have gotten smaller and faster, new technologies and structural innovations to existing technologies have emerged to cope with the technical demands of today's applications, such as CMOS FinFETs for highly scaled digital applications, III-V platforms for high-speed and high-voltage applications, and silicon-germanium (SiGe) BiCMOS for performance-constrained analog and RF applications.

The attractiveness of SiGe BiCMOS technologies stems from the ease of integration with existing CMOS platforms with little overhead cost. This allows for the design and fabrication of high-performance monolithic mixed-signal circuits and systems. Designers can use SiGe HBTs for high-performance analog and RF applications, while at the same time leveraging the highly scaled CMOS for dense digital circuitry.

SiGe HBTs enjoy a 2-3 generational advantage over Si Field Effect Transistors (FETs) in terms of f_T/f_{MAX} performance. This means that a SiGe HBT fabricated at 130 nm lithographic node will have equal or greater performance to an nFET fabricated in a 65 nm [4]. For a fixed lithography node, SiGe BiCMOS will have greater performance than regular CMOS, making them significantly cheaper.

Another attractive quality about SiGe HBTs is their potential use in electronics for extreme environments. These include high temperatures, low temperatures, wide temperature ranges, radiation active environments, among others. SiGe HBTs have

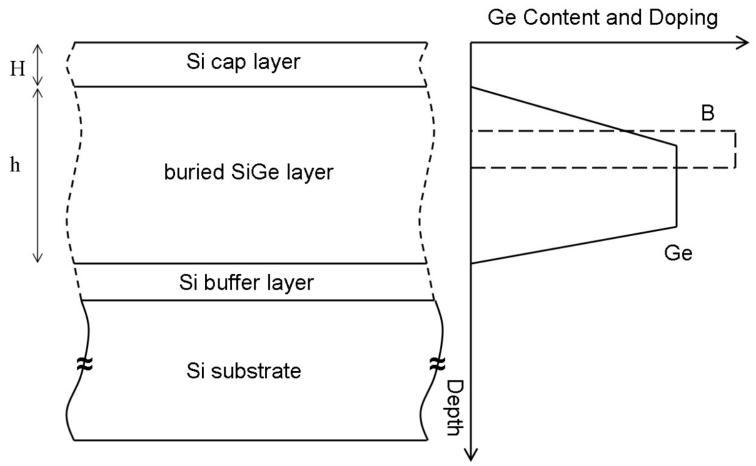


Figure 1: Schematic epitaxial SiGe film used in SiGe HBTs (after [1]).

been shown to be a viable option for cryogenic applications [5]. In addition, they are also tolerant to total ionizing dose effects to multi-Mrad levels, making them attractive for radiation active environments [6].

1.1 Silicon Germanium Technology

Silicon (Si) and Germanium (Ge) have the same crystallographic structure, with Ge having a lattice constant that is 4.18% larger than that of Si. The lattice constant of SiGe alloys follows Vegard's rule to the first order,

$$a(Si_{1-x}Ge_x) = (1-x)(a_{Si}) + x(a_{Ge}) \tag{1}$$

where a is the lattice constant and $0 > x > 1$ is the Ge fraction. $Si_{1-x}Ge_x$ alloys grown on Si substrates will experience compressive strain, since their lattice constant will be larger than that of Si for any value of $x > 0$. This lattice mismatch imposes a constraint on the maximum thickness of a pseudomorphic heteroepitaxial layer. If the thickness of this layer exceeds the critical thickness of stability, the strain will be relaxed through the formation of misfit dislocations, which are not desirable for high-yielding device applications [7].

A deposited SiGe film actually consists of three layers, as shown in Figure 1: a

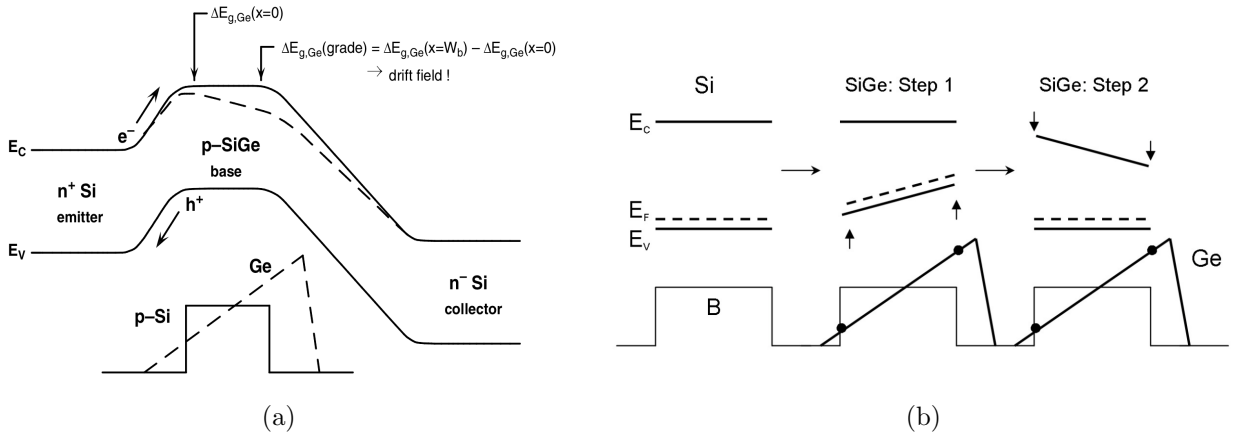


Figure 2: (a) Band diagram of a Si BJT (solid lines) and a SiGe HBT with a graded Ge profile in the base (dashed lines) under forward active bias. (b) Diagram showing the changes due to the introduction of Ge in a p-type base of an *npn* BJT. (after [1]).

thin, undoped Si buffer layer; a boron-doped SiGe active layer; and a thin, undoped Si cap layer. The Si buffer layer helps to ensure a pristine growth surface for the SiGe film. It can also be used in device design to decrease the junction field and increase the breakdown voltage of the transistor [8]. The SiGe layer has a varying Ge concentration and an embedded boron doping spike (for *npn* devices). The Si cap layer not only provides a Si termination for the SiGe alloy, which is important in oxidation steps, but also helps with overall film stability. In addition, the intrinsic layer can be used to reduce emitter-base (EB) junction field, reducing parasitic tunneling current.

There are various techniques that can be used to grow SiGe films including rapid thermal chemical vapor deposition (RTCVD), molecular beam epitaxy (MBE) and ultrahigh vacuum chemical vapor deposition (UHV/CVD), among others [7].

1.2 Theory of Operation of SiGe HBTs

In a SiGe HBT, the Ge content is linearly graded from 0% near the metallurgical EB junction to some peak value near the collector-base (CB) junction and then rapidly ramped down to 0%. The resulting band diagram for a SiGe HBT biased in the forward active region is shown in Figure 2a (in dashed lines) and is compared to that

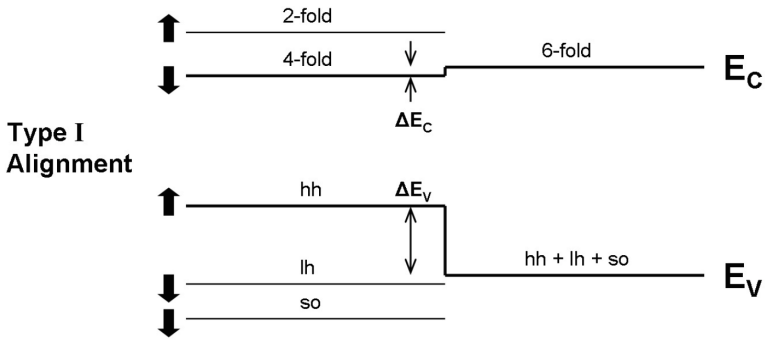


Figure 3: Schematic band alignment of strained SiGe grown on Si substrate (after [1]).

of a similar Si BJT (in solid lines) for the same applied bias.

It is important to mention that strained SiGe layers have positive ΔE_C and ΔE_V with respect to the Si substrate, with ΔE_V, being larger. This is known as type-I band alignment and is shown in Figure 3. Linear grading of the Ge content in the SiGe base will cause a gradual shift in the valence band energy as shown in Figure 2b. However, because the base is doped with acceptors, the difference between the Fermi-level and the valence band energy ($E_F - E_V$) is fixed. For a device in equilibrium, E_F must be constant across the structure. This leads to an effective bending in the conduction band as shown in Step 2 of Figure 2b.

Note that for *pnp* devices, where the difference ($E_C - E_F$) is constant, this Ge profile will result in a notch in the valence band at the CB junction, which will lead to trapping of holes and reduce device performance. Although there are commercial complementary SiGe processes [2, 9, 10], profile design and optimization for *pnp* devices is an active area of research [11, 12]. Throughout this paper, we will focus on the operation and performance of *npn* devices, but refer interested readers to [7] and [1] for more information on the challenges of designing SiGe *pnp* devices.

Similar to a Si BJT, when a voltage is applied between the base and emitter terminals, electrons are injected across the EB potential barrier. These carriers diffuse

across the base and are swept by the built-in electric field of the reverse-biased CB junction into the collector. This applied bias also produces back-injection of holes from the base into the emitter. Normally, the emitter is heavily doped with respect to the base, which would make the density of back-injected holes small compared to the electrons injected into the base, yielding a finite current gain (β).

One of the primary effects of introducing Ge in the *dc* operation of the device is an increase of collector current density (J_C). The derivation of an expression for J_C is not trivial, since we must take into account a non-constant bandgap material in the base. For a detailed solution to this problem, the reader is referred to [13]. An expression for J_C has been derived in [1] and is given by,

$$J_{C,SiGe} \simeq \frac{qD_{nb}}{N_{ab}^{-}W_b}\left(e^{qV_{BE}/kT}-1\right)n_{io}^{2}e^{\Delta E_{gb}^{app}/kT}\cdot\left\{\tilde{\gamma}\tilde{\eta}\frac{\Delta E_{g,Ge}(grade)}{kT}e^{\Delta E_{g,Ge}(0)/kT}\right\} \quad (2)$$

where q is the electron charge, D_{nb} is the electron diffusivity, N_{ab}^{-} is the acceptor concentration in the base, W_b is the base width, V_{BE} is the applied base-emitter voltage, k is the Bolztmann constant, T is the temperature, n_{io} is the low-doping intrinsic carrier density for Si, ΔE_{gb}^{app} is the heavy-doping-induced apparent bandgap narrowing in the base region, $\tilde{\gamma}$ is the average "effective density of states ratio" between SiGe and Si, $\tilde{\eta}$ is the minority electron diffusivity ratio between SiGe and Si, $\Delta E_{g,Ge}(grade)$, is the bandgap narrowing in the base due to the graded Ge, and $\Delta E_{g,Ge}(0)$ is the bandgap offset due to the Ge concentration at the EB junction.

Although there are many parameters in this expression, there are a few important things that we can highlight. First, note how the current is an exponential function of the Ge content at the EB junction. As we increase this value, we are lowering the EB potential barrier for electron injection, as shown in Figure 2a. This leads to an exponentially higher amount of electron injection for a given base-emitter voltage (V_{BE}). Since the emitter regions of the Si BJT and SiGe HBT are essentially the same, the base current density (J_B), will be roughly the same [14]. This results in an increased current gain $\beta = J_C/J_B$. This increase in J_C and β can be observed in

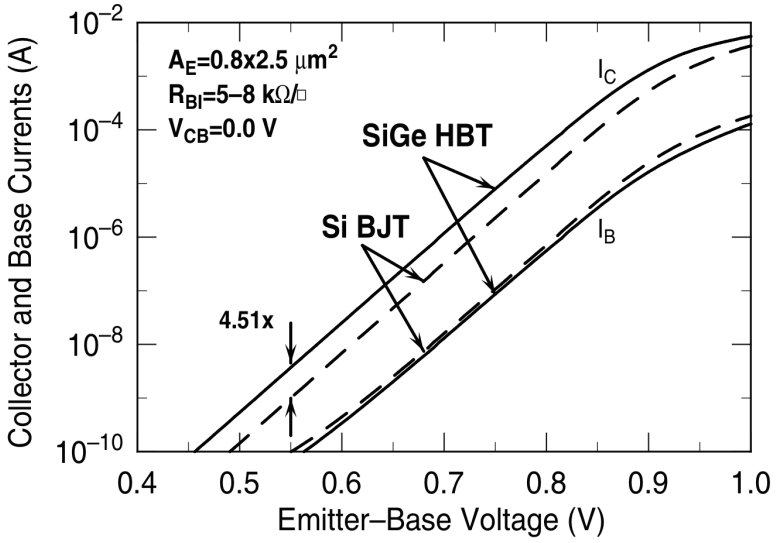


Figure 4: Gummel plot for a SiGe HBT (solid lines) and a comparable Si BJT (dashed lines) (after [1]).

Figure 4 which shows a Gummel plot for a SiGe HBT (solid lines) and a comparable Si BJT (dashed lines).

Another benefit of the added Ge is an exponential increase in the early voltage (V_A) which is directly related to the output conductance of the device ($\partial I_C/\partial V_{CE}|_{V_{BE}=const}$). Figure 5 shows the relationship between V_A and the output conductance of a transistor. From a circuit design perspective, a low output conductance (i.e. infinite output resistance or infinite V_A) is desired, since this means that the output current is independent of the output voltage. However, as we increase the collector-base voltage (V_{CB}), the CB junction becomes more reverse-biased, increasing the depletion region width, which narrows the neutral base width (W_b) and gives rise to an increase in J_C. In SiGe HBTs, the triangular Ge profile effectively "weights" the base profile making it harder to deplete the neutral base [1]. Figure 6 shows a plot of $V_{A,SiGe}/V_{A,Si}$ across temperature. Note that the ratio is always greater than one, which means that the Early voltage for a SiGe HBT is higher than that for a comparable Si BJT. This makes it a more ideal current source since its output conductance is lower, i.e. the output resistance is higher.

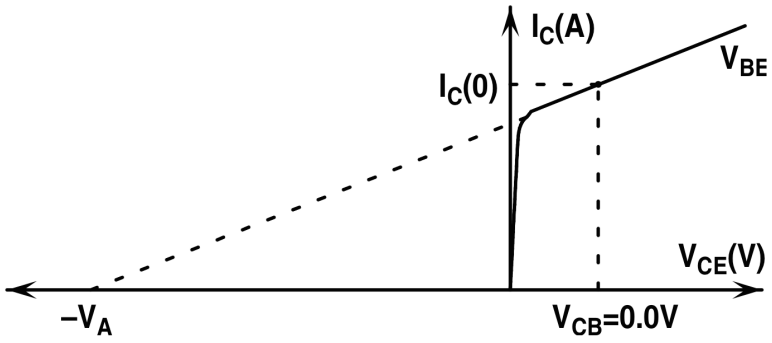


Figure 5: Schematic representation of the relationship between Early voltage and a transistor's output characteristics (after [1]).

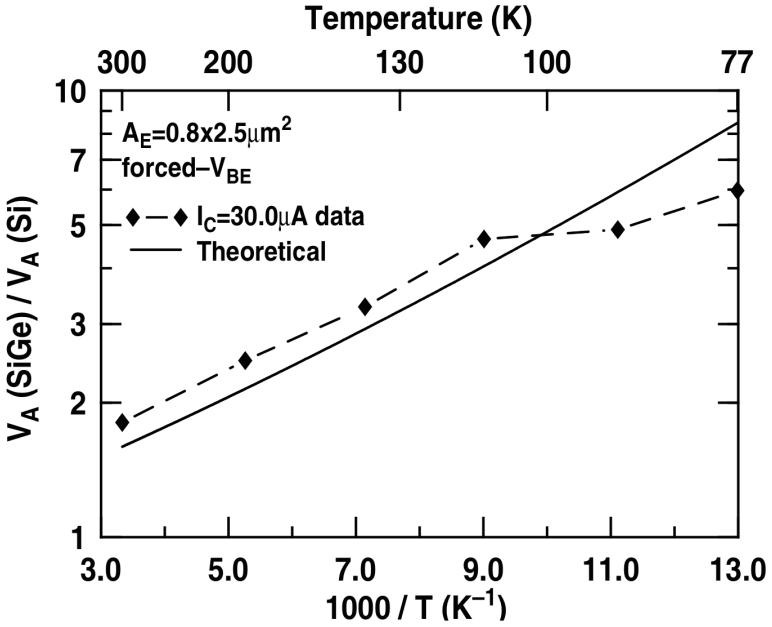


Figure 6: Ratio between Early voltage for SiGe HBT and comparable Si BJT (after [1]).

The grading of Ge also induces a built-in quasi-drift field in the neutral base given by $(\Delta E_{g,Ge}(x = W_b) - \Delta E_{g,Ge}(x = 0))/W_b$. This electric field aids carrier transport by adding a drift component to the minority carriers in the base, which reduces the base transit time τ_B. In Si BJTs, τ_B is typically the limiting factor in the unity-gain frequency (f_T), which is given by,

$$\frac{1}{2\pi f_T} = \tau_{EC} = \tau_E + \tau_C + \tau_B + \tau_{CSCL} \tag{3}$$

where τ_E, τ_C and τ_{CSCL} are the emitter, collector and collector space charge layer/region (SCR) transit times, respectively.

The emitter transit time τ_E is reciprocally related to the *ac* β of the transistor [14]. As previously discussed, the Ge profile in the base increases β, which reduces τ_E. Although this value is not a limiting factor in f_T in most technologies, it will become important as we push the vertical scaling of these devices to their ultimate limit.

Another important figure of merit is the maximum oscillation frequency f_{MAX}, which is given by,

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}} \tag{4}$$

where R_B is the *ac* base resistance and C_{BC} is the collector-base capacitance. For most circuit applications a value of $\beta = 100$ would be sufficient. The increase in β due to the added Ge allows us to trade some of this current gain for a lower base resistance by increasing the base doping, which will ultimately increase f_{MAX}.

1.3 Radiation Effects in HBTs

Radiation can have adverse effects in the operation of electronic components. This is not only a concern for in-orbit or deep-space applications, but also for terrestrial applications [15]. There are three major types of radiation-induced damage: 1) total ionizing dose effects (TID), 2) displacement damage (DD), and 3) single event effects. The following section provides a cursory explanation of each of these effects, as well as some approaches to mitigate radiation-induced damage.

1.3.1 Total Ionizing Dose

Total ionizing dose (TID) effects are cumulative, and are a result of energy deposition in insulating materials, which can degrade device and circuit performance. When ionizing radiation deposits energy in an insulator and generates electron-hole pairs,

the electric field across the insulator will tend to separate these charges. Since electrons have higher mobility than holes, they tend to be swept away by the electric field, leaving holes trapped in the insulator. Over time, these holes can diffuse to the insulator-semiconductor interfaces and result in interface traps. Some notable effects of these traps are threshold voltage shifts and off-state leakage current increase in MOSFETs. Increases in off-state leakage could be harmful to digital circuit, since the current required from the power supply will continue to increase with dose.

SiGe HBTs enjoy an increased robustness to TID, and are said to be tolerant to multi-Mrad(SiO_2) dose levels [6]. Their built-in TID tolerance is a result of the device structure required to deposit the SiGe allow in the base. The main effect of TID on SiGe HBTs is an increase in base leakage current and a reduction in current gain at low injection. This is a result of interface traps generated along the E-B spacer. However, for most high-performance circuits, these devices are biased above the point where the leakage current is significant and its effect is typically not observed in circuit performance.

1.3.2 Displacement Damage

Displacement damage (DD) effects are a result of a particle with mass penetrating the semiconductor material and losing energy through non-ionizing mechanisms. This can result in the incident particle physically displacing atoms in the semiconductor lattice, which could lead to point defects [16]. These defects could lead to increased recombination centers that can increase leakage current in devices. Furthermore, if the displaced atom is a dopant species that forms an interstitial defect, this dopant will no longer be electrically active. This effect is known as dopant deactivation and can cause shifts in device performance. Due to the relatively high doping levels in SiGe HBTs, DD effects are not the limiting factor in their radiation response.

1.3.3 Single Event Effects

A single-event effect (SEE) occurs when an ionized, high-energy particle penetrates a semiconductor material. As it passes through, the particle transfers its energy to the material and creates electron-hole pairs along its path. The generated carriers can then be separated by the internal electric fields of active devices, generating a current that can have adverse effects on the circuit operation. These effects are typically transient in nature, and although often non-destructive, they are still of interest to the space community as they can alter the proper operation of systems or compromise the data acquired by a scientific instrument. A notable example of a non-destructive effect that caused a temporary malfunction in a spacecraft and loss of scientific data is NASA's Microwave Anisotropy Probe (MAP), in which the microprocessor was reset due to a radiation-induced transient signal [17]. Examples of these types of effects include: single-event transients (SETs), in which the current generated in the material exits through the device terminals and propagates through the circuit or system; and single-event upsets (SEUs), in which a bit in a digital system is flipped from a logic high to a logic low or vice versa.

There are some instances in which SEEs could be catastrophic, and can result in permanent damage to the devices or circuits affected. Examples of these effects include: single-event latchup (SEL), in which a positive feedback is established in a thyristor structure and can lead to device destruction if not contained; single-event burnout (SEB), in which a power FET is forced into thermal runaway that could also lead to device destruction; and single-event gate rupture (SEGR), in which the gate dielectric of a FET ruptures due to an excessively high electric field during a transient event [18].

Although SiGe HBTs are robust against TID and DD effects, they are particularly susceptible to SEEs, in particular, to single-event transients. When a heavy-ion passes through the emitter-base-collector stack, the high-density of carriers generated in this

region will effectively break down the built-in electric fields in the junctions, making them behave like resistive components, and leading to large current transients at the device terminals. In addition, any transient occurring outside this emitter-base-collector stack but inside the deep trench (DT) isolation will lead to charge collection by the reverse-biased sub-collector to substrate junction [6]. Since the collector is typically the output for most circuits, this effect is also of concern for proper circuit operation. A recent study suggests that the germanium-induced quasi-drift field in the SiGe base plays a significant role in the SET response of SiGe HBTs, and has shown that increasing Ge content in the base increases the observed transients at the device terminals [19].

1.3.4 Mitigation Approaches

Aside from typical shielding mechanisms employed by spacecraft designers to mitigate the effects of radiation on the system, there are two main approaches for making electronic systems radiation tolerant or "rad-hard": radiation hardening by design and radiation hardening by process.

1.3.4.1 Radiation Hardening By Design

Radiation hardening by design (RHBD) approaches encompass a broad range of techniques that utilize changes in design procedure to mitigate the effect of radiation on electronic systems. These include changes in device layout, circuit topologies, system implementations, and software architecture [20].

A common RHBD approach for digital circuits is the use of triple-module redundancy (TMR). In this approach, all logic paths are triplicated and are connected to a majority voter circuit that decides the appropriate logic value. It is extremely unlikely that a single heavy-ion event would corrupt two logic paths simultaneously, and this approach has been used to demonstrate a radiation tolerant shift register in a SiGe HBT process [21].

Radiation hardening techniques can also be implemented at the system level [22]. For example, SEL can be mitigated and prevented from being catastrophic by placing current monitors on all power supplies and power-cycling the system if an excessively (but still safe) amount of current is drawn. In addition, identifying the functional impact of an SEE and the associated risk and criticality can be used to place SEE design requirements on particular subsystems. Using parity-checks, data retransmission, active watchdog timers are all examples of system- and software-level radiation hardness.

1.3.4.2 Radiation Hardening By Process

The alternative to RHBD techniques is radiation hardening by process (RHBP), in which the semiconductor fabrication process is altered to reduce the adverse effects of radiation. An example of this is the use of silicon-on-insulator (SOI) processes to prevent single-event latchup, since the parasitic thyristor structure often present in CMOS processes would be removed. However, changes in process to mitigate a particular effect on a given mission could be costly. Therefore, an RHBD approach is often preferred.

1.4 Complementary SiGe HBT Platforms

Throughout the years, the performance of *npn* SiGe HBTs has been steadily increasing. These efforts have resulted in a 0.7 THz device unveiled last year by the Innovations for High Performance Microelectronics (IHP) [23]. Unfortunately, *pnp* SiGe HBTs have not enjoyed the same performance increases. Designing high-speed *pnp* devices can be challenging, primarily due to the reduced mobility of holes compared to electrons, and the valence band offsets between Si and SiGe which could introduce significant heterojunction barrier effects (HBEs). However, having matched-performance *npn* and *pnp* devices in the same process is desirable as it enables a number of circuit topologies not available with only *npn* devices and can significantly reduce the power

consumption of bipolar circuits [24].

The fastest commercially-available complementary SiGe process is a third-generation platform by IHP [2]. This complementary bulk SiGe:C BiCMOS process features 0.25 μm matched *npn* and *pnp* devices with a peak f_T/f_{MAX} of 110 GHz/180 GHz and 90 GHz/120 GHz, respectively [25]. This process uses a novel collector structure for increased performance that removes the shallow trench isolation between the emitter and collector. In addition, the process also removes deep trench (DT) isolation, to improve heat dissipation [26]. A schematic cross-section view of the complementary devices in this process are shown in Fig. 7.

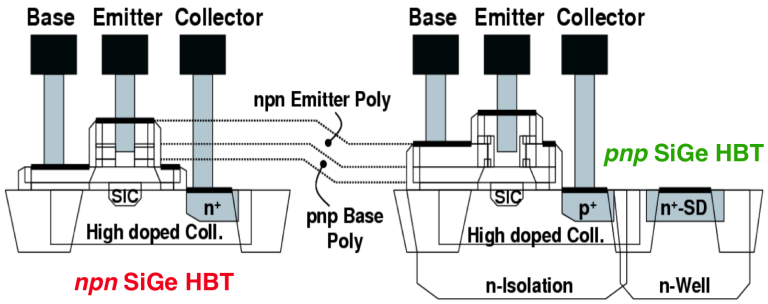


Figure 7: Schematic cross-section of the IHP SG25H3P *npn* and *pnp* SiGe HBT (after [2]).

Previous work using a pulsed-laser source has shown that bulk *pnp* SiGe HBTs exhibit a smaller transient peak, shorter duration, and reduced sensitive area compared to *npn* devices [27]. This improved single-event transient response has been attributed to the n-well isolation required to fabricate *pnp* devices in a complementary (*npn* + *pnp*) SiGe platform. In addition, devices from this particular process have been shown to be resistant to TID [28]. However, little work has been done on assessing the circuit-level response of this process. The main goal of the present work is to assess the single-event response of this complementary SiGe BiCMOS platform in the context of analog, RF and digital circuits.

CHAPTER II

SINGLE-EVENT TRANSIENT RESPONSE OF COMPARATOR PRE-AMPLIFIERS

The results in this chapter have been published in the following article [3]: A. Ildefonso, N. E. Lourenco, Z. E. Fleetwood, M. T. Wachter, G. N. Tzintzarov, A. S. Cardoso, N. J. H. Roche, A. Khachatrian, D. McMorrow, S. P. Buchner, J. H. Warner, P. Paki, M. Kaynak, B. Tillack, and J. D. Cressler, Single-Event Transient Response of Comparator Pre-Amplifiers in a Complementary SiGe Technology, *IEEE Trans. Nucl. Sci.*, vol. 64, pp. 8996, Jan. 2017.

2.1 Introduction

Voltage comparators are ubiquitous in applications requiring analog-to-digital conversion. Latched comparators are particularly useful for analog-to-digital converters (ADC) as they save the state of the comparator at a known point in time, thereby allowing for higher accuracy. Single-event transients in comparators have been known to cause malfunctions in several spacecraft, including NASA's Microwave Anisotropy Probe (MAP), in which the microprocessor was reset due to a transient at the output of an LM139 comparator [17]. Although this malfunction did not result in mission failure, it resulted in the loss of scientific data and is an example of the importance

of designing robust and reliable circuits for radiation-intense space applications.

Silicon-germanium heterojunction bipolar transistors (SiGe HBTs) have improved *ac* and *dc* performance compared to their silicon counterparts, with modest cost overhead, making them ideal for performance-constrained analog, high-speed digital, and RF applications. In addition, their performance enhancement at low temperatures and their built-in tolerance to total ionizing dose (TID) exposure (up to several Mrad(SiO_2)), makes them suitable for many space applications. However, SiGe HBTs are known to be susceptible to single-event effects (SEEs), and in particular to single-event transients (SETs). Therefore, finding ways to mitigate radiation-induced transients at the device and circuit level is an active area of research.

It is difficult to define and quantify SET driven errors in purely analog applications; however, comparators are an exception since they are usually followed by a digital circuit, typically a latch or flip flop. In this case, the latch defines a transient peak and duration threshold for which an analog SET will generate erroneous data that will propagate through the digital system. For high-speed digital and mixed-signal circuits, such as a latched comparator, the magnitude of the peak is critical since it can induce bit-flips, or single-event upsets (SEU) [6], as opposed to a small peak with long duration which will not induce bit-flips if it remains below the logic trigger threshold.

SiGe silicon-on-insulator (SOI) platforms have been shown to reduce the SET duration due to the suppression of the long diffusion mechanism present in transients induced in bulk technologies [29]. However, though the magnitude of the transient peak is similar for comparable bulk and SOI platforms. Using SOI platforms to mitigate the SET response can be a costly solution. Therefore, it is desirable to find alternatives in SiGe bulk technologies.

Previous work has shown that bulk *pnp* SiGe HBTs exhibit a smaller transient peak, shorter duration, and reduced sensitive area compared to *npn* devices [27].

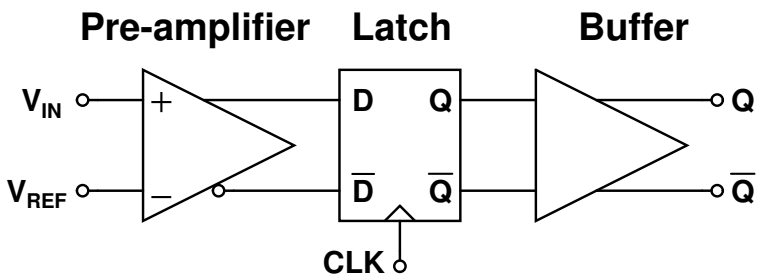


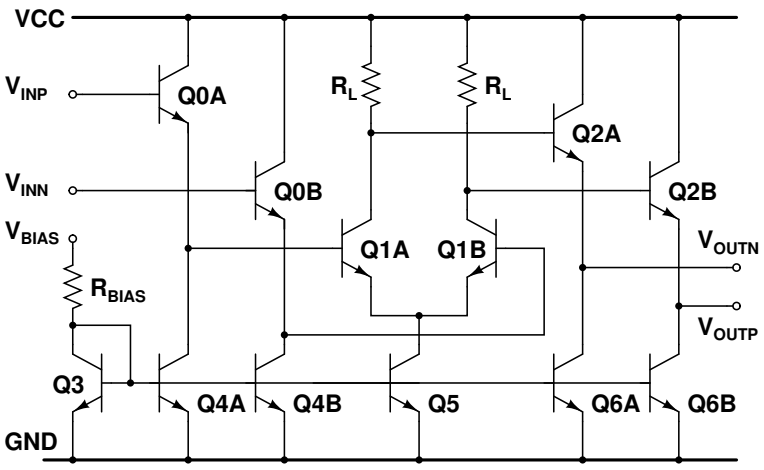
Figure 8: Simplified schematic of a latched comparator architecture.

This improved SET response has been attributed to the n-well isolation required to fabricate *pnp* devices in a complementary (*npn* + *pnp*) SiGe platform. In addition, devices from this particular process have been shown to be resistant to TID [28]. However, little work has been done to assess the radiation robustness of bulk SiGe *pnp* devices within actual analog circuits.

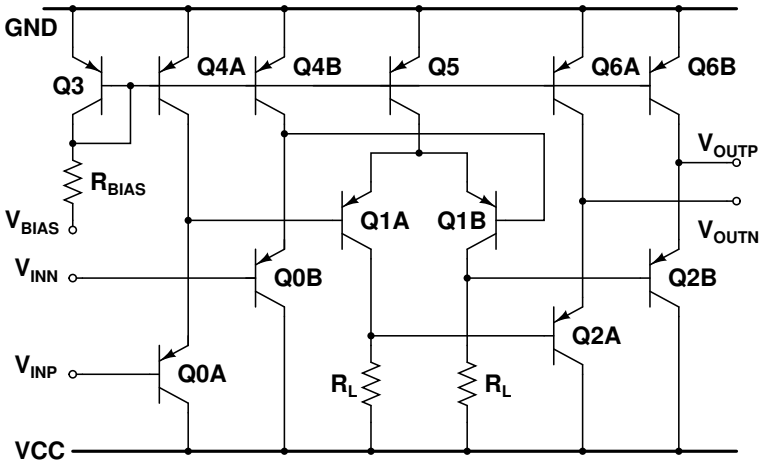
This chapter investigates the SET response of the pre-amplifier stage in a latched comparator designed with the topology shown in Fig. 8. Two circuits were designed, using either only *npn* or only *pnp* devices to facilitate a direct comparison between the two device types. An SEU-hard latch has been previously demonstrated in SiGe technology by employing radiation hardening by design (RHBD) techniques [21]. However, any large transients presented at the input of the latch that have been produced by the pre-amplifier stage will be latched directly on the clock edge, potentially storing erroneous data. Therefore, reducing the transient magnitude at the output of the pre-amplifier below the logic threshold of the following latch is desired.

2.2 Circuit Description

Two fully-differential comparator pre-amplifiers with the same topology were designed, one only using *npn* devices and the other only using *pnp* devices, as shown in Fig. 9. The circuits were fabricated on the SG25H3P third-generation platform by Innovations for High Performance (IHP) Microelectronics [2]. This complementary bulk SiGe:C BiCMOS process features 0.25 μm matched *npn* and *pnp* devices with



(a) *npn* Comparator



(b) *pnp* Comparator

Figure 9: Simplified schematic of the designed comparator pre-amplifiers using (a) only *npn* devices and (b) only *pnp* devices.

a peak f_T/f_{MAX} of 110 GHz/180 GHz and 90 GHz/120 GHz, respectively [25].

Since each differential circuit is symmetric, only half of the signal path was irradiated. To facilitate the discussion, equivalent transistors in the schematic (e.g., Q0A and Q0B) will simply be referred to by their instance number (e.g., Q0), unless further distinction is necessary.

In the schematic shown in Fig 9, Q0 forms a Darlington pair with Q1, which increases the input resistance by $\approx \beta + 1$. Q1A and Q1B form the resistive-load differential pair that steers current between one of two branches, depending on the

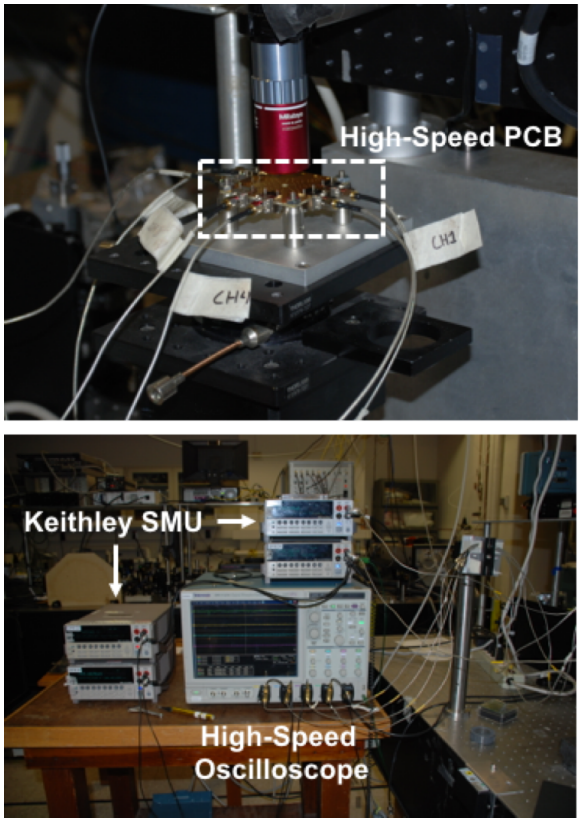


Figure 10: Experimental setup at the Naval Research Laboratory

differential input. Q2 serves as an output buffer and level shifter for the following stage. Q3, together with R_{BIAS}, sets the circuit bias current, which can be tuned by changing V_{BIAS}. Q4–Q6 serve as biasing transistors, mirroring the current flowing through Q3.

Both circuits were designed to produce the same output swing of ±200 mV, which translates to them having the same small-signal gain [30]. The *pnp* comparator was designed to operate with a negative supply, and the n-well isolation of all devices is tied to ground (i.e., the highest potential).

2.3 Experimental Setup

Laser-induced transients were measured at the U.S. Naval Research Laboratory (NRL) using through-wafer two-photon absorption (TPA) [31]. TPA carrier injection allows for time-resolved, position-dependent three-dimensional measurements of single-event

transients (SETs). The system features 150 fs, 1260 nm wavelength optical pulses at a repetition rate of 1 kHz with a 0.88 μm full-width-at-half-maximum (FWHM) focused spot size. The samples were attached and wire-bonded to a custom-designed printed circuit board (PCB) that exposes the backside of the die for irradiation. SETs were captured using a high-bandwidth real-time oscilloscope. The experimental setup is shown in Fig. 10.

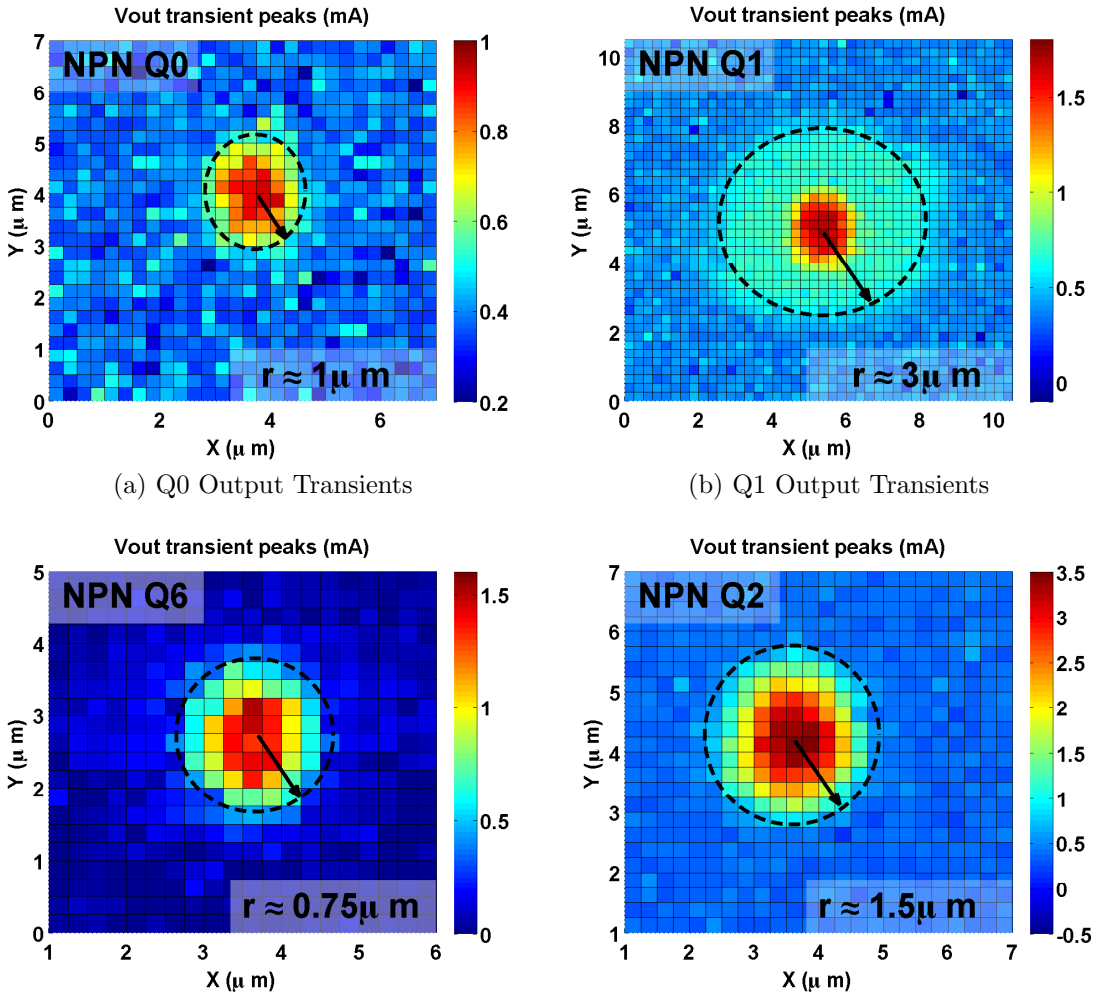
2.4 Experimental Results

2.4.1 Sensitive Area

2-D raster scans for all devices in a particular signal path, including all bias transistors, were performed on both circuits using a differential input voltage of $v_{id} = 0$ V, a laser pulse energy of 2.6 nJ, and a step size of 0.25 μm. This bias point was chosen in order to reduce the differential output noise component by using a single supply to bias both inputs. A lower output noise floor allows us to measure smaller transient peaks that would otherwise be lost, resulting in a clearer picture of the sensitive area of each device. Fig. 11 and Fig. 12 show 2-D raster scans depicting the magnitude of the output current transient peaks of several devices for the *npn* and *pnp* comparators, respectively, when the output is taken differentially. To obtain the differential current, the measured differential output voltage (i.e. $V_{OUTP} - V_{OUTN}$), has been divided by the input impedance of the oscilloscope (i.e. 50 Ω). Note that the intensity color scale is the same between equivalent *npn* and *pnp* devices. Scans for the remaining transistors have been omitted for brevity, but show the same trends as noted in the following discussion.

The data show that the output transient peaks induced in the comparator designed using only *pnp* devices are smaller compared to those in the *npn* version. Ideally, the sensitive area of each device would be defined as the area where transient magnitudes are large enough to affect the comparator's decision. However, a modest laser pulse

energy was chosen to avoid stressing the circuits, and induced transients are not large enough to meet this criterion. Therefore, in this work, the sensitive are has been defined as the region with transient magnitudes ≥ 0.5 mA. This area has been delimited by a dashed ring in Figs. 11 and 12. From these figures, it can be seen that the sensitive area for the *pnp* devices is consistently smaller compared with that of the equivalent *npn* devices, by amounts ranging between 44–80%, depending on the irradiated device. This is consistent with previous findings when individual devices from this technology were irradiated [27]. These transient measurements show that although the sensitive area for each device varies depending on their location on the circuit, *pnp* devices still have the advantage, in terms of having a smaller sensitive area, when measured in a circuit application. This is a significant result.



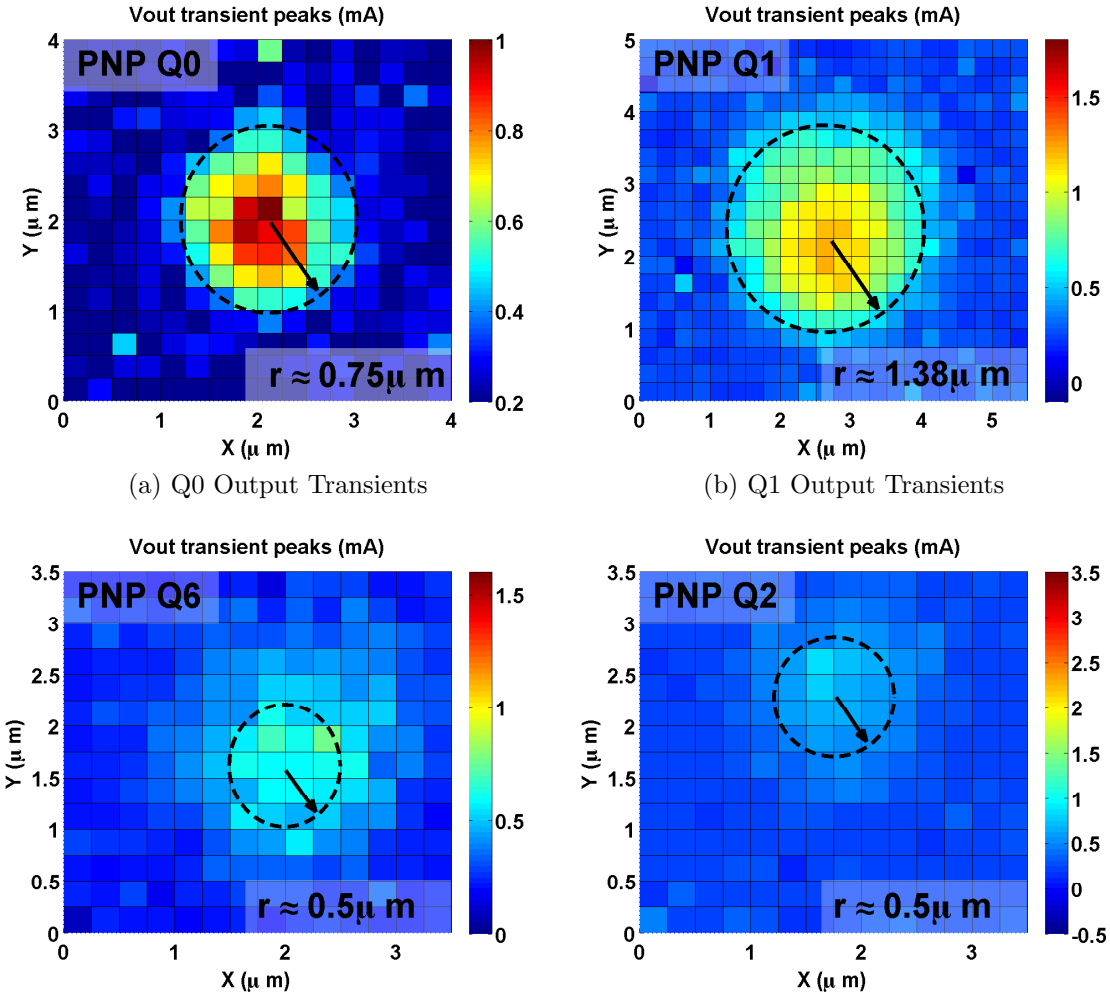
(a) Q0 Output Transients

(b) Q1 Output Transients

(c) Q6 Output Transients

(d) Q2 Output Transients

Figure 11: Measured 2-D output current transient peaks when the output is taken differentially and the specified transistor in the *npn* comparator is struck with the laser. The dashed ring delimits the area of the device with transient magnitudes ≥ 0.5 mA for a laser pulse energy of 2.6 nJ.



(a) Q0 Output Transients

(b) Q1 Output Transients

(c) Q6 Output Transients

(d) Q2 Output Transients

Figure 12: Measured 2-D output current transient peaks when the output is taken differentially and the specified transistor in the *pnp* comparator is struck with the laser. The dashed ring delimits the area of the device with transient magnitudes ≥ 0.5 mA for a laser pulse energy of 2.6 nJ.

2.4.2 Input Voltage Dependence

In addition to 2-D raster scans, voltage sweeps were also performed on the individual devices. To accomplish this, the laser was focused on the most sensitive part of the device (i.e., the spot that produced the maximum transient peak) and the differential input voltage was swept by maintaining V_{INN} at a fixed value and sweeping V_{INP}, such that $v_{id} = V_{INP} - V_{INN}$. The laser energy was set to 0.9 nJ for all voltage sweeps in order to avoid stressing the circuit. These sweeps prove useful in determining whether a particular device will corrupt the output of a comparator. For example, if v_{id} is negative, then the differential output voltage v_{out} will also be negative and any negative transients will not corrupt the comparator decision. Fig. 13 shows the theoretical sensitive operating regions of the comparator. If $v_{id} \ll 0$, negative transients will not affect the output and only positive transients larger than the V_{IL} of the following latch will be strong enough to corrupt the output. A similar analysis can be made for $v_{id} \gg 0$. However, for small v_{id}, small transients can upset the output if the current through the core differential pair is not completely switched to one branch of the circuit. This analysis can be used to identify sensitive devices within the circuit.

Fig. 14 shows the measured peak transient amplitudes when the output is taken differentially for the common-mode devices, Q3 and Q5, in the *npn* comparator. As expected, when $v_{id} = 0$ V, the transient peak is approximately zero, since both signal paths will carry the same transient and will cancel once the difference is taken at the output nodes. However, as v_{id} is swept, the output transient peaks resemble the sigmoidal characteristic output curve of a comparator, since the transient is being steered to one side of the circuit. When Q5 is struck, the generated transient current, i_{SET}, will flow through the active branch of the differential pair, further lowering the output voltage at that node by $i_{SET} \times R_L$. When Q3 is struck, the transient current will lower the base voltage of all the bias transistors by $i_{SET} \times R_{BIAS}$, including Q5. This

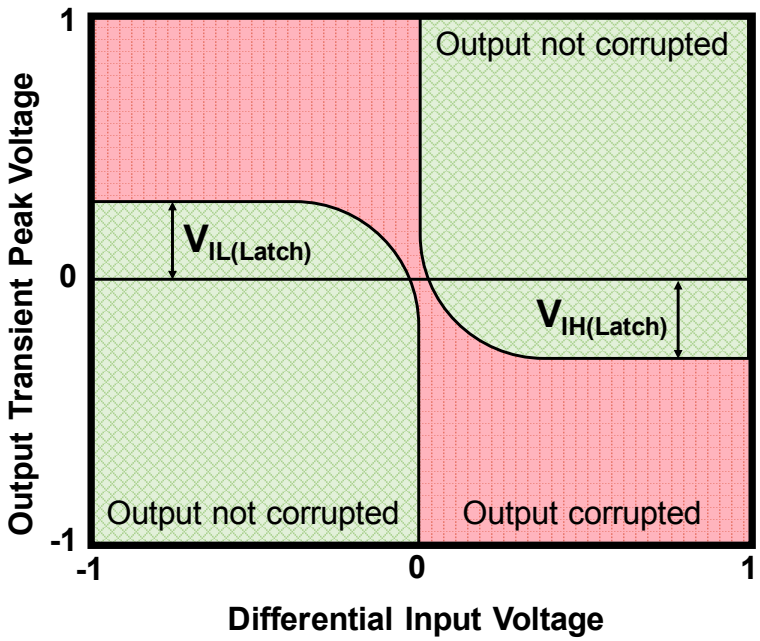


Figure 13: Sensitive operating region of a comparator for given output transient polarities.

will reduce the current through the active branch of the differential pair, increasing the output voltage at that node. The same conclusions can be obtained for the *pnp* comparator and the corresponding plots have been omitted for brevity.

According to this analysis, when Q5 is struck, the resulting transient will not affect the comparator's decision since the sign of the transient is the same as that of the output voltage. However, when Q3 is struck, the resulting transient has the opposite polarity of the output voltage, resulting in a potential corruption of the data. For mitigation, emitter degeneration resistors can be added to the bias transistors in order to reduce the transient peak [32].

Fig. 15 shows the measured peak transient amplitudes when the output is taken differentially, for the devices in one of the differential signal paths (from V_{INP} to V_{OUTN}) in the *npn* comparator. Referring back to Fig. 13, it can be seen that all of the transients produced by these devices may corrupt the comparator decision at certain input signal values.

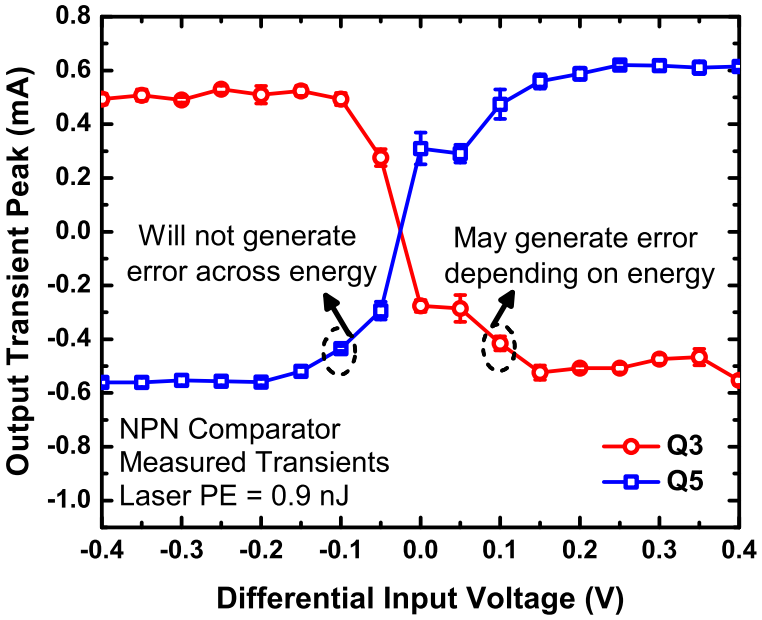


Figure 14: Measured differential output current transient peaks as a function of differential input voltage when the common-mode devices in the *npn* comparator are struck with a laser pulse energy of 0.9 nJ.

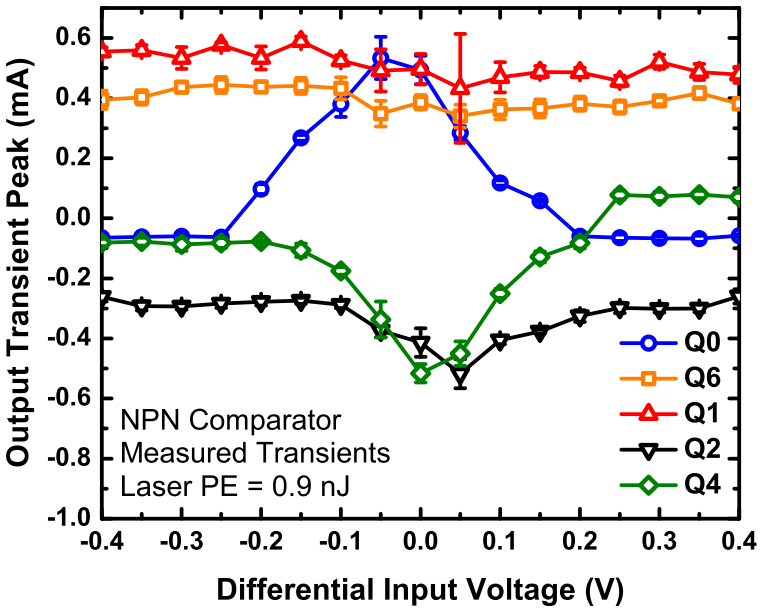


Figure 15: Measured differential output current transient peaks as a function of differential input voltage when devices on one of the signal paths in the *npn* comparator are struck with a laser pulse energy of 0.9 nJ.

Transients generated by strikes on Q2 and Q6 will have a smaller voltage dependence than other devices on the circuit. Since Q2 serves as a buffer, with a relatively high resistance at the emitter (from the collector resistance of Q6), its bias point does not change dramatically with input voltage. Furthermore, since emitter transients are positive, differential output transients ($V_{OUTP} - V_{OUTN}$) will be all negative or all positive for Q2A and Q2B strikes respectively. In a similar manner, since Q6 is a bias transistor, and its collector is connected directly to the output, there will be very little voltage dependence on the transients. In addition, since collector transients have a negative polarity, differential output transients will be all positive or all negative for Q6A and Q6B strikes respectively. This qualitative analysis is confirmed by the data in Fig. 15.

Transients generated by striking the remaining transistors do not follow the trend expected when applying circuit theory. One would expect that, for a given energy, the output peaks would change polarity as the input voltage is increased, since the transient current would be steered to one branch of the circuit. However, for a low enough energy, when Q1 is conducting all or none of the tail current provided by Q5, the small voltage increase at the base of Q1 due to a transient generated at Q0 will have negligible effect on the current flowing through Q1, blocking the transient from reaching the output.

This analysis was confirmed by performing voltage sweeps at different laser energies. Figs. 16 and 17 show strikes at Q0 and Q4, respectively, for laser pulse energies ranging from 1 nJ to 9 nJ. Both plots show the same trend. At low energies, the transient response deviates from the expected sigmoid, while at higher energies the response becomes as expected. This interpretation has been further confirmed by performing ion-strike Technology Computer-Aided Design (TCAD) simulations, as discussed in the following section.

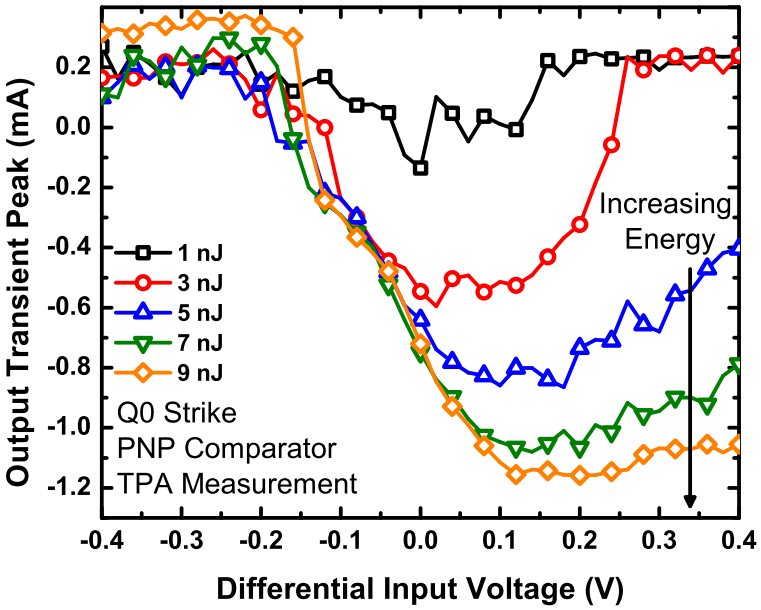


Figure 16: Measured differential output current transient peaks for a laser strike on Q0 in the *pnp* comparator as a function of input voltage and laser pulse energy.

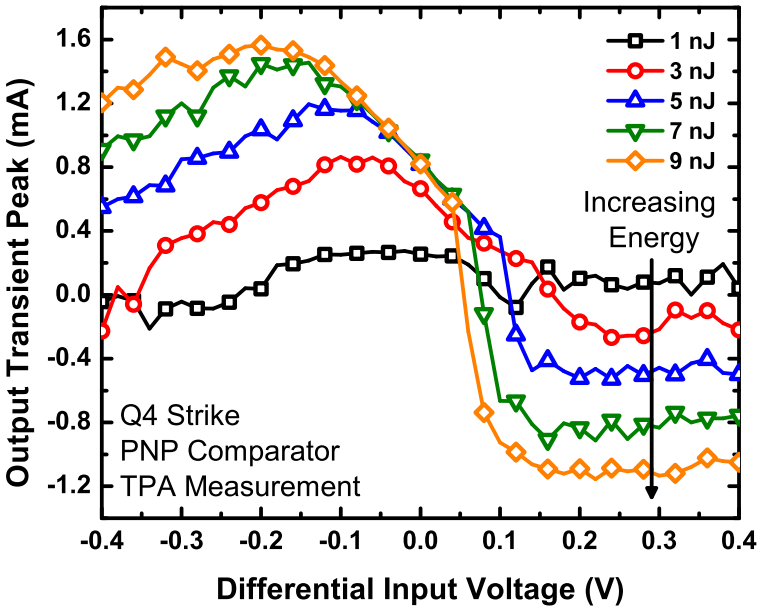


Figure 17: Measured differential output current transient peaks for a laser strike on Q4 in the *pnp* comparator as a function of input voltage and laser pulse energy.

2.5 TCAD Modeling

TCAD models have been developed using the Synopsys TCAD suite and calibrated to match the *dc* characteristics of the Cadence IHP SG25H3P process design kit (PDK) compact models. Circuit-level ion-strike simulations have been performed in order to study the propagation of SETs through different nodes in the circuit when a particular device is struck. This allows us to identify the most sensitive nodes in the circuit and potentially apply RHBD approaches to limit the transient peaks to below the logic threshold of the following latch.

In order to validate the change in trend for voltage sweeps at very low laser energies, mixed-mode heavy-ion-strike TCAD simulations at different linear energy transfers (LETs) were performed. Fig. 18 shows the simulated differential output transient peak as a function of input voltage for a Q0 strike on the *npn* comparator across multiple LETs. The figure not only shows larger peaks, but also different trends with varying input voltage as the energy is increased, confirming our experimental result. This change in trend should be considered when performing hardness assurance testing, as the intended application will ultimately determine the sensitivity regions of the comparator (e.g., high input voltages versus low input voltages).

2.5.1 Input Voltage Dependence

In order to evaluate the transient response of each circuit as a function of input voltage, heavy-ion-strike TCAD simulations were performed at an LET of 10 MeV-cm^2/mg for various input voltages. This LET was chosen since it was high enough for the circuit to exhibit the expected sigmoidal transient response for several devices. As shown in Fig. 13, a sigmoidal shape of transient peaks as a function of input voltage that has opposite polarity to the comparator's characteristic would be the worst-case scenario. Fig. 19 shows the transient peaks when the output is taken differentially as a function of input voltage. In some of these cases, the magnitude of the transient peaks for

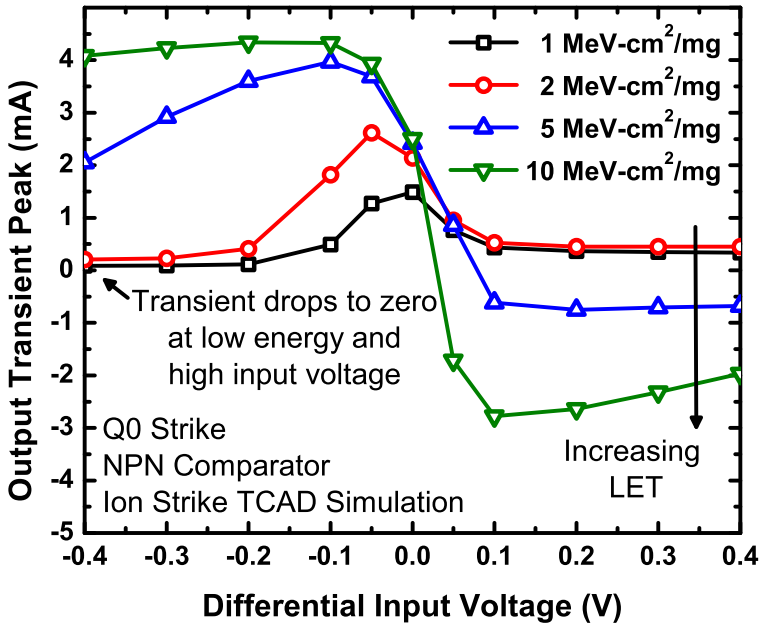
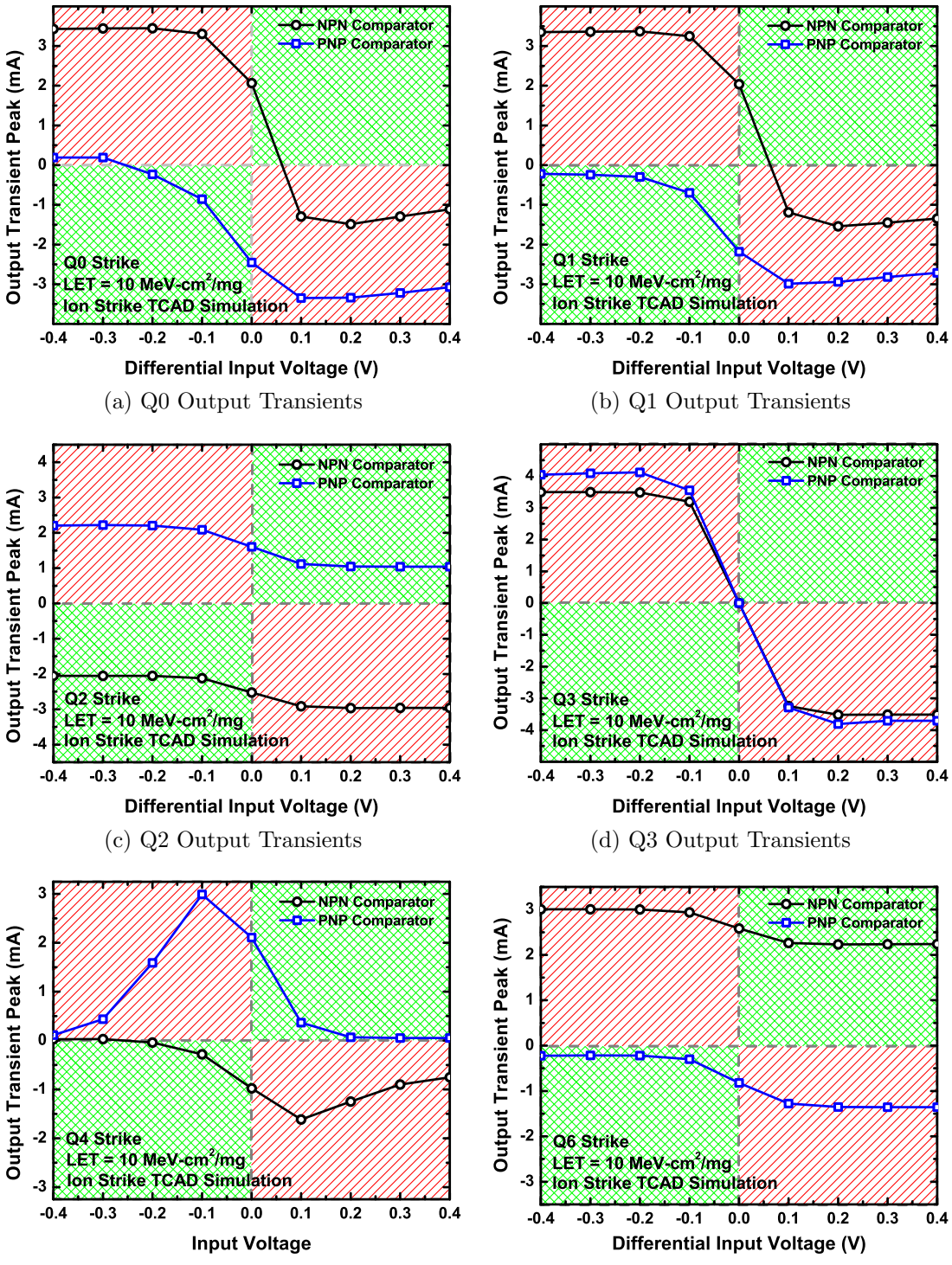


Figure 18: Simulated output current transient peaks for a heavy-ion strike on Q0 in the *npn* comparator as a function of input voltage and LET.

$v_{id} > 0$ are larger for the *pnp* devices than the *npn* devices. The increase in magnitude can be attributed to the fact that the struck *pnp* device is in the "off" state, while the equivalent *npn* device is in the "on" state, which results in worse transients for the *pnp* devices. The opposite can be said for $v_{id} < 0$. Therefore, directly comparing transient peaks for a single specific input results in an unfair comparison.

As previously discussed, transients will not corrupt the output when the polarity of the transient agrees with the polarity of the output voltage. However, if the generated transient and the output voltage have different polarities, this does not necessarily mean that the output will be corrupted, since the transient would need to have a certain magnitude, determined by the logic thresholds of the following stage, for the output to be corrupted. For this reason, rather than stating whether there will be an error or not, we have defined a metric to quantify the relative severity of transients generated in the *npn* devices when compared to their *pnp* counterparts. The metric integrates the transient peaks as a function of input voltage, when the sign of the transient peaks and the input voltage are opposite. This metric, σ, can be represented



(a) Q0 Output Transients

(b) Q1 Output Transients

(c) Q2 Output Transients

(d) Q3 Output Transients

(e) Q4 Output Transients

(f) Q6 Output Transients

Figure 19: Simulated output current transient peaks for a heavy-ion strike as a function of input voltage for an LET of 10 MeV-cm^2/mg. The red quadrant with diagonal lines indicates the region where the output of the comparator might be corrupted, while the green quadrant with crosshatch pattern indicates the region where the output of the comparator will not be affected.

Table 1: Values of metric σ for each device

Device	σ *npn*	σ *pnp*
Q0	8.80	6.47
Q1	8.76	5.60
Q2	5.79	4.21
Q3	11.97	13.21
Q4	2.33	3.07
Q6	5.87	2.54
Total	43.52	35.10

mathematically as,

$$\sigma = 100 \int \left[\frac{1 - \mathrm{sgn}(v_{in}) \times \mathrm{sgn}(T(v_{in}))}{2} \right] \times |T(v_{in})| \mathrm{d}v_{in} \tag{5}$$

where v_{in} is the input voltage, $T(v_{in})$ is the transient peak for a given input voltage, and $\mathrm{sgn}(x)$ is the signum function, which equals 1 for $x > 0$, -1 for $x < 0$, and 0 for $x = 0$. The metric is scaled by 100, in order to obtain more manageable numbers. This metric could be interpreted as an indicator of relative vulnerability of output corruption due to SETs. Since no explicit logic level was assumed, it does not favor one circuit over the other. Note that this metric purposefully does not take sensitive area into account in order to decouple the the SET response due to different input voltages from the already improved SET response resulting from the smaller sensitive area of the *pnp* devices.

The metric was applied for transients obtained from all the devices in the circuit, except for Q5, since it was determined earlier that transients generated from this device would not corrupt the output. The values of σ obtained for each device are shown in Table 1. The σ value for all of the *pnp* devices, except Q4 and Q3, is smaller than the *npn* devices. The σ values can be added for each device to obtain a circuit-level σ. At the circuit level, the resulting σ, shown at the bottom of Table 1, is 21.4% smaller for the *pnp* circuit than for the *npn* circuit. This result reinforces the fact that the *pnp* circuit will have an improved SET response.

2.5.2 Impact on Error Cross Section

The data presented show that a single point can't be used to establish the impact of an SET on the operation of the comparators, or to compare two different topologies. For example, in Fig. 19, although transients for Q4 are worse for the *pnp* comparator, by calculating the cumulative σ for the circuit, it is shown that the *pnp* circuit still outperforms the *npn* version.

Error cross sections are produced by counting the amount of errors obtained for a particular fluence of heavy-ion strikes and normalizing to circuit area across various LETs. Fig. 20 shows the differential output transient peaks for heavy-ion strikes on the devices of both circuits as a function of LET for an input voltage of 0 V. The plot shows increasing transient peaks as a function of increasing energy, as expected. From this simulation, one can expect the σ values for both circuits to increase as the heavy-ion energy is increased.

In this technology, both *npn* and *pnp* devices have the same area, and therefore both circuits will have very similar area. We have presented laser data that shows that the sensitive area of the *pnp* devices is smaller compared to their *npn* counterparts. This means that, for a given heavy-ion energy, there is a lower probability of generating a transient of a given peak for the *pnp* devices.

We can interpret σ as a value indicating the relative energy required to produce an upset (the lower the σ, the higher energy required for upset). If we now couple these two results, and assume equal probability of striking each device, then it can be concluded that the *pnp* circuits will have a higher LET threshold (due to the lower circuit σ) and a reduced error cross section (due to the reduced sensitive area). This establishes *pnp* devices as a viable RHBD approach for various applications.

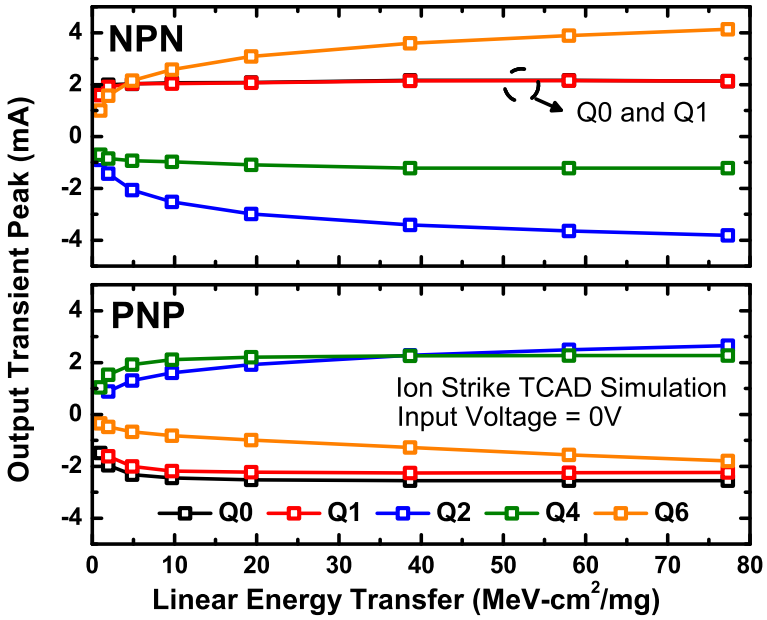


Figure 20: Simulated output current transient peaks as a function of LET.

2.6 Summary

We have shown, both through experimental data and TCAD simulations, that the comparator designed using *pnp* devices enjoys the same reduced sensitive area and transient peaks as a single device, when compared to their *npn* counterparts. Experimental data show that *pnp* devices in the studied circuit exhibit a reduced sensitive area by amounts ranging between $44-80\%$. In addition, the *pnp* comparators show a reduced sensitive operating region with respect to input voltage by 21.4%, according to the metric, σ, previously defined.

It is difficult to say, without a specific application and further experimentation, that using *pnp* devices will result in completely radiation-hardened circuits. However, the improved SET response of *pnp* devices over their *npn* counterparts suggests that designing circuits using *pnp* devices will require less aggressive RHBD techniques. In addition, introducing *pnp* devices to a circuit designer's toolkit, can enable unique topologies of radiation-hardened circuits that have not yet been explored in the field of bipolar circuits.

CHAPTER III

SINGLE-EVENT TRANSIENT RESPONSE OF LOW-NOISE AMPLIFIERS

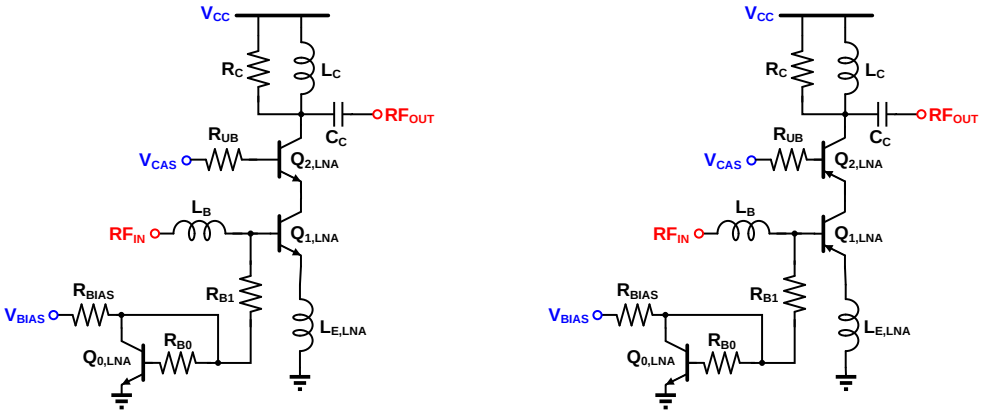
3.1 Introduction

Low-noise amplifiers (LNAs) are ubiquitous components in receiver circuits, which are necessary in any type of in-orbit communications payload. Ensuring the robustness of the communications system in a spacecraft is crucial, since failure of this system might compromise the mission. Furthermore, these systems are subject to data corruption due to heavy-ion-induced, or single-event, transient signals generated in the active devices that propagate through the receiver chain. This could result in the corruption of a command sent to the spacecraft from the base station, which could have adverse effects. Therefore, it is relevant to find ways to mitigate single-event transients in these circuits.

As shown in the previous chapter, one approach is to design circuits using *pnp* devices, as they showed a reduced SET response compared to circuits designed using *npn* devices. For the presented analog circuits, the reduction in SET response came at no cost to performance, since these circuits operate at lower frequencies. However, the *ac* performance of the *npn* and *pnp* , although "matched," is not identical. This could lead to differences in circuit performance as the frequency of operation is increased. In this chapter, the trade-off between the performance of an RF circuit, specifically an LNA, and its single-event transient response is explored through the use of mixed-mode TCAD simulations.

3.2 Design Procedure

Two single-stage cascode LNAs with the same topology were designed, one only using *npn* devices and the other only using *pnp* devices, as shown in Fig. 21. The circuits were designed on the SG25H3P third-generation platform by Institute of High Performance (IHP) Microelectronics [2]. This complementary bulk SiGe:C BiCMOS process features 0.25 μm matched *npn* and *pnp* devices with a peak f_T/f_{MAX} of 110 GHz/180 GHz and 90 GHz/120 GHz, respectively [25]. The *pnp* LNA was designed to operate with a negative supply and all N-well connections are tied to ground (i.e., the highest potential).



(a) *npn* Low-Noise Amplifier (b) *pnp* Low-Noise Amplifier

Figure 21: Schematic of the designed low-noise amplifiers using (a) only *npn* devices and (b) only *pnp* devices.

To allow for a fair comparison between both circuits, they were designed for simultaneous power and noise matching using the methodology in [33]. Although this methodology might not yield the best circuit in terms of any single performance metric, and additional circuit design techniques could be employed to improve the designs, it was chosen for this work because it provides an algorithmic path for design that results in LNAs with decent performance. It ensures that both circuits were designed using the same procedure to allow for a direct comparison between the

resulting performance. The design procedure is specified in the following text.

Selecting Current Density First, the optimum collector current density ($J_{C,opt}$) that ensures minimum NF_{min} must be selected, for equally sized devices in the cascode structure. A one-finger minimum-sized ($0.84 \times 0.22\ \mu m^2$) device was selected for each case and the V_{BE} of the lower device in the cascode core was swept. The maximum achievable gain (MAG) and minimum achievable NF (NFmin) are plotted as a function of J_C in Fig. 22. Note from Fig. 22, that for the both designs, significantly higher LNA gain can be achieved by biasing at a higher collector current density with a marginal increase to NF. However, for the purposes of this comparison, the value for $J_{C,opt}$ (i.e., minimum NFmin) was selected for both cases. The values for $J_{C,opt}$ for *npn* and *pnp* cascode cores, are 425.43 $\mu A/\mu m^2$ and 383.28 $\mu A/\mu m^2$, respectively.

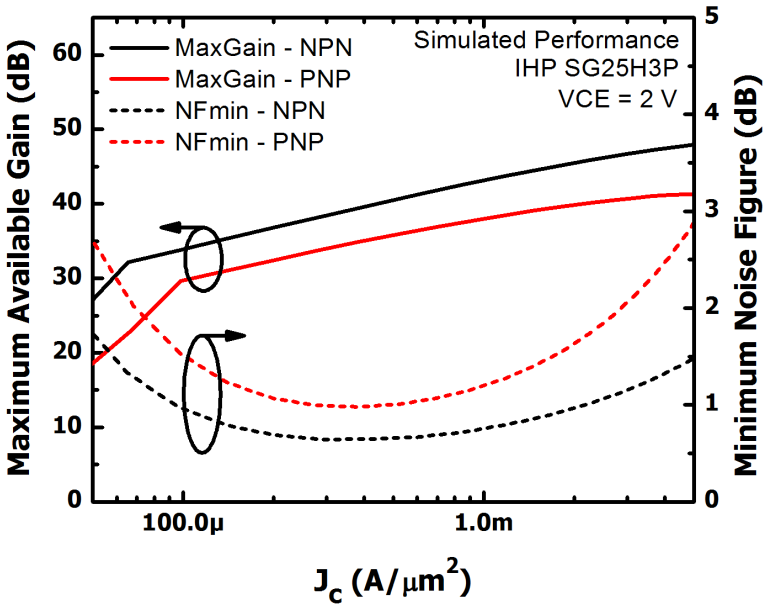


Figure 22: Maximum available gain and minimum achievable noise figure as a function of collector current density.

Selecting Device Size The emitter lengths of the cascode devices should be scaled so that the optimum source resistance ($R_{S,opt}$) is close to 50 Ω while maintaining the J_C selected in the previous step. In this process, both the emitter width and the

emitter length are fixed, therefore parallel devices must be used. The optimum source resistance for noise matching of a single transistor is given by

$$R_{s,opt} = \frac{f_T}{f}\sqrt{\frac{2r_b}{J_C \times A_E}\frac{kT}{q}} \tag{6}$$

where f_T is the cutoff frequency of the device, f is the operating frequency, J_C is the current density at which the device is biased, A_E is the total emitter area, and r_b is the base resistance. From the equation, it can be observed that by increasing the total emitter area, or in this case, the number of parallel devices, the optimum source resistance can be decreased. Fig. 23 shows $R_{S,opt}$ as a function of the number of parallel devices for the *npn* and *pnp* cascode structure. Note that for the *pnp* cascode, less parallel devices are required to achieve 50 Ω due to the fact that this device has lower f_T. The selected dimensions for the *npn* and *pnp* devices were 44 and 40 respectively, as they were closest to 50 Ω and were feasible in layout by using devices with multiple fingers. The *npn* cascode core was implemented by using 4 11-finger devices, while the *pnp* core was implemented using 5 8-finger devices, since 8-fingers was the maximum available for *pnp* devices.

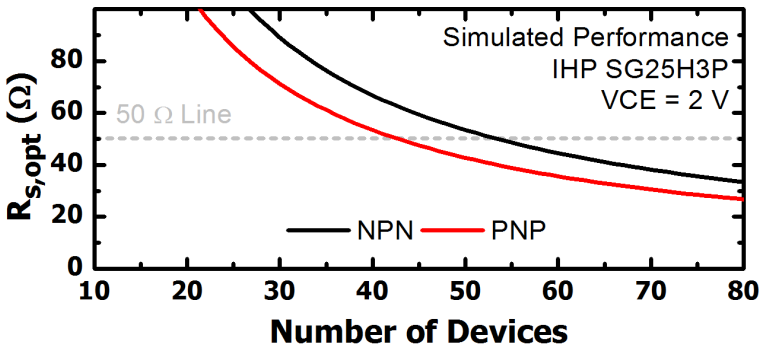


Figure 23: Optimum source resistance for noise matching as a function of number of parallel devices.

Selecting Emitter Degeneration Inductor The emitter degeneration inductor (L_E) is selected to match the real part of the input impedance. The value of L_E is

given theoretically by

$$L_E = \frac{50}{2\pi f_T} \tag{7}$$

where f_T is the cutoff frequency of cascode structure, for the selected emitter lengths biased at the selected J_C. Although this equation gives a good estimate of the required inductance, the resulting value changes once the layout is implemented. Therefore, the cascode cores were laid out using Cadence Virtuoso and the layout with extracted parasitics was used for simulation in Keysight's Advanced Design System (ADS) via Dynamic Link. An S-parameter simulation was performed, where the value of L_E was swept until the real part of the input impedance was matched to 50 Ω. This resulted in values L_E of around 500 pH and 850 pH for the *npn* and *pnp* designs respectively.

Selecting Series Base Inductor The series base inductor, L_B, is selected to cancel the reactive part of the input impedance. It is given theoretically by

$$L_B = \frac{1}{\omega^2 C_{BE}} - L_E \tag{8}$$

where ω is the operating frequency, C_{BE} is the base-emitter capacitance of the bottom device in the cascode structure, and L_E is the emitter inductor selected in the previous step. This equation is again different once the layout is implemented due to the series inductance and shunt capacitance introduced by the vias and metal transitions. Therefore, the value of L_B was chosen by sweeping L_B in an S-parameter simulation until the reactive component of the input impedance was canceled. This resulted in L_B values of around 3.3 nH and 2.8 nH for the *npn* and *pnp* designs, respectively.

Adding a Collector Resistor Because the output impedance of the cascode structure is high, output matching can be very difficult. A collector resistor can be added to, not only ease output impedance matching, but also to improve stability, at the cost of reducing peak gain. For both designs, a collector resistor of 400 Ω was chosen as it resulted in reasonable inductor values for output matching.

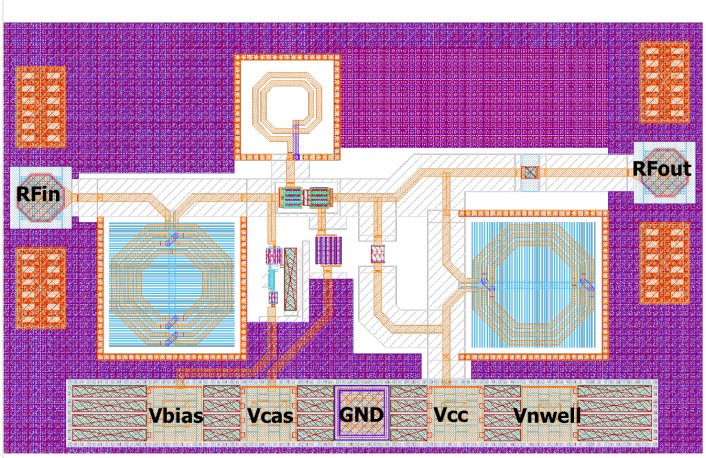
Implementing Output Match The output impedance matching is realized by using an L-network with a shunt inductor (L_C) and a series capacitor (C_C). These values were selected in the same way as the other inductors in the circuit. The values for L_C were around 3.3 nH and 2.1 nH for the *npn* and *pnp* designs respectively. The series capacitors, which also serve as a DC block for the following stage, resulted in values of 340 pF for both designs.

Finalizing Design The cascode core was biased using a current mirror with ratio 1:4 for the *npn* LNA and 1:5 for the *pnp* LNA. The bias resistors, R_{B1} and R_{B0} were designed to also have these ratios to correct for differences in base current between the core and the current mirror. A 10 Ω resistor was added on the upper-base node of each circuit to improve stability. Stability of both circuits was verified using the S-Probe technique, also known as the Gamma-Probe technique [34]. Both circuits were laid out using Cadence Virtuoso. The final layout for each circuit is shown in Fig. 24.

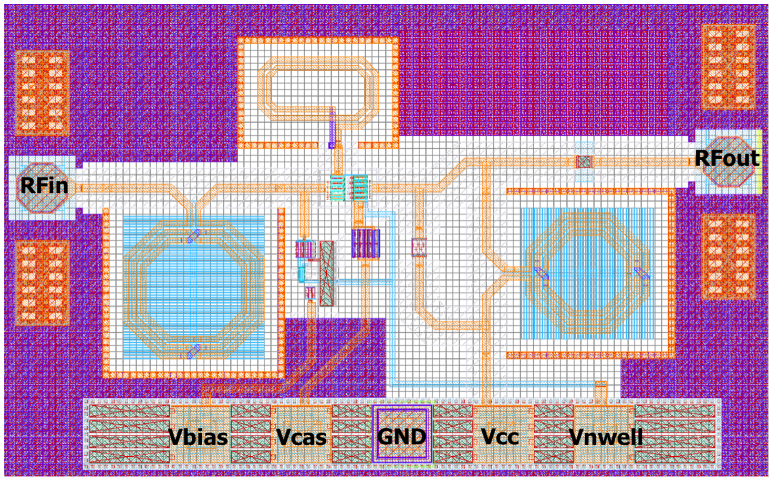
3.3 Simulated Performance

After the layout design was complete, the circuit performance was simulated using Keysight's ADS. For the results shown in these simulations, all inductors and capacitors were EM simulated using Sonnet, and the layouts with extracted parasitics were used for all active devices, resistors and chip pads.

The simulated S-parameters of the designed circuits are shown in Fig. 25. Both circuits achieve an input and output return loss (S_{11} and S_{22}, respectively) lower than 10 dB at the center frequency, and a reverse isolation (S_{12}) greater than 30 dB across the simulated frequencies. The main differences between both designs lie in the gain (S_{21}). Using the same design procedure, the *npn* LNA achieved a gain of 14.93 dB, while the *pnp* LNA achieved a gain of 10.74 dB. This result is not surprising since the maximum available gain of the *npn* LNA core at the selected bias, was larger



(a) *npn* Low-Noise Amplifier



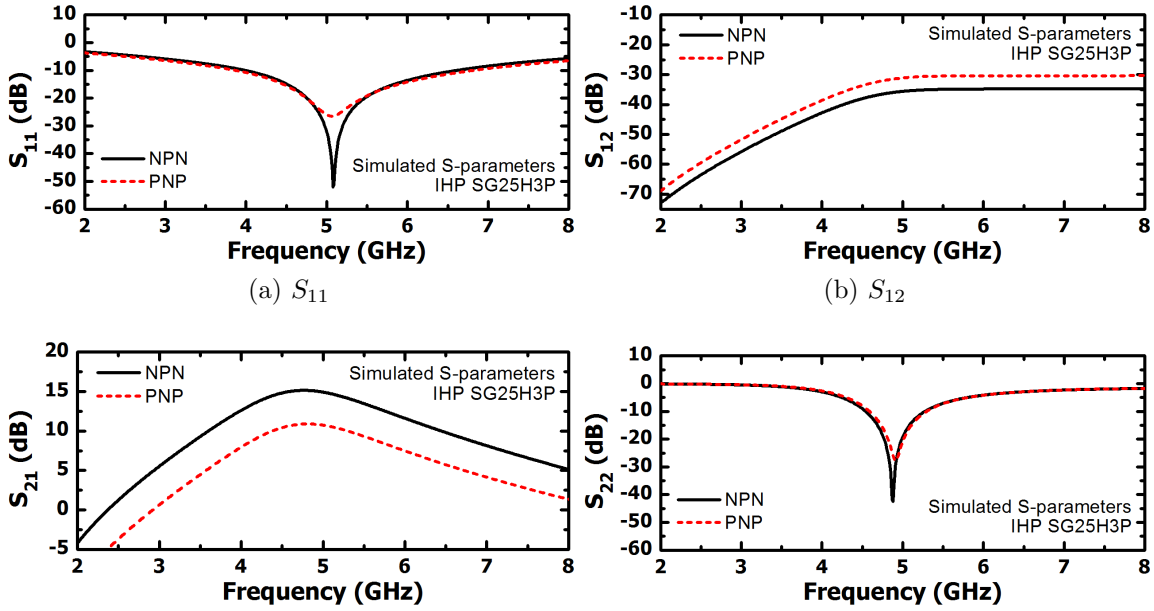
(b) *pnp* Low-Noise Amplifier

Figure 24: Cadence Layout of the designed low-noise amplifiers using (a) only *npn* devices and (b) only *pnp* devices.

than that of the *pnp* core. However, even though the *pnp* LNA has lower gain, it also shows a lower input-referred P1dB compression point, as shown in Fig. 26.

The noise figure (NF) performance as a function of frequency is shown in Fig. 27. The *npn* LNA shows a NF of 1.62 dB at 5 GHz, while the *pnp* LNA shows a NF of 2.13 dB at the same frequency. This is a difference of 0.51 dB, which is consistent with the 0.55 dB difference in NFmin at the selected bias currents.

While the *npn* design shows higher performance in almost every metric, it also consumes more *dc* power with a total of 7.87 mW compared to 5.55 mW for the *pnp*



(a) S_{11} (b) S_{12}

(c) S_{21} (d) S_{22}

Figure 25: Comparison of simulated S-parameters for the designed low-noise amplifiers.

design. A summary of the performance of both circuits are shown in Table 2. It is worth noting that, although some of these metrics could be greatly improved by selecting a different topology, bias, or layout scheme, the purpose of this study is to obtain decent performing circuits that were designed following the same procedure.

Table 2: LNA Performance Summary.

Specification	*npn* LNA	*pnp* LNA
Layout Area	0.69 × 1.12 mm^2	0.72 × 1.14 mm^2
Center Frequency	5 GHz	5 GHz
Noise Figure at 5 GHz	1.62 dB	2.13 dB
Gain (S_{21}) at 5 GHz	14.93 dB	10.74 dB
Input P1dB	-16.25 dBm	-17.39 dBm
Supply Voltage	2 V	-2 V
P_{DC}	7.87 mW	5.55 mW

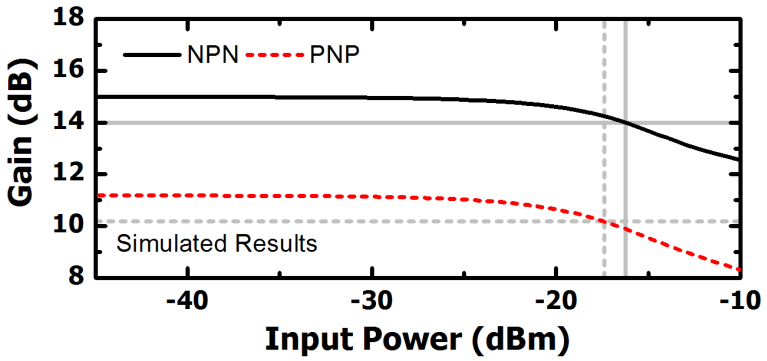


Figure 26: Comparison of simulated single-tone linearity for the designed low-noise amplifiers.

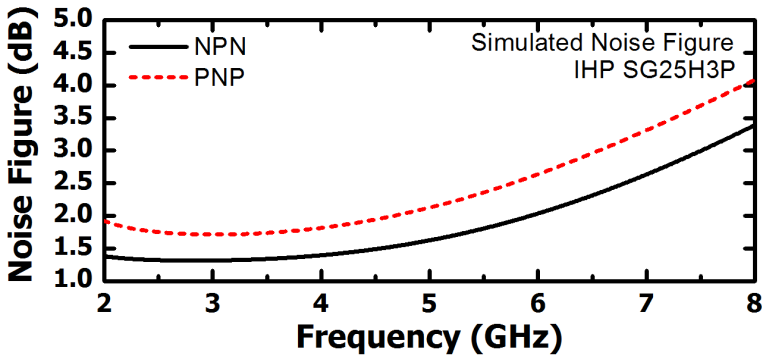


Figure 27: Comparison of simulated noise figure for the designed low-noise amplifiers.

3.4 Heavy-Ion Strike Simulations

TCAD models have been developed using the Synopsys TCAD suite and calibrated to match the *dc* characteristics of the Cadence IHP SG25H3P process design kit (PDK) compact models. These models were used for mixed-mode heavy-ion simulations. In this type of simulation, a physics-based transistor model is placed in a circuit netlist. The circuit equations and physics-based device equations are solved simultaneously. Although the models are not accurate enough to capture the exact circuit performance (e.g., gain, noise figure, input return loss, etc.), simulations can be performed with no RF input to obtain general trends in the SET response of these designs.

In these simulations, both the input and output were terminated with 50 Ω, and the produced transients are measured at the output node of the amplifiers. Fig. 28

shows the output transient for both designs when a heavy ion with an energy of 10 MeV-cm^2/mg passes through the common-emitter device of each LNA. The data show a 1.9x reduction in transient peak for the *pnp* heavy-ion strikes compared to strikes on equivalent *npn* devices. Note that the resulting decrease in transient peak is not a result of the reduce gain in the *pnp* LNA. During a heavy-ion strike, the struck device is flooded with carrier densities that are comparable to the doping levels in the device. Therefore, typical transistor behavior is not expected during this time. It is important to mention that the transients produced by each circuit will have a similar shape but opposite polarity due to the change in power supply polarity. In Fig. 28, the polarity of the *npn* SET has been inverted.

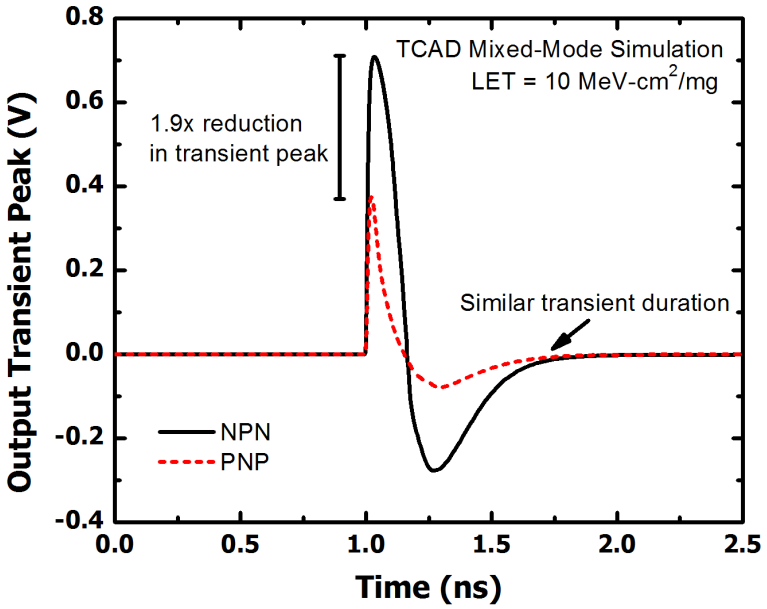


Figure 28: Comparison of single-event transient captured at the output of the low-noise amplifiers when a heavy ion with an energy of 10 MeV-cm^2/mg passes through the common-emitter device.

To explore the effects of heavy-ion energy on the produced SETs, the LET was swept in simulation. All heavy-ion-induced transients had a similar shape to that shown in Fig. 28, and their individual plots have been omitted for brevity. Fig. 29 shows the absolute value of the maximum transient peak as a function of LET. As

expected, the peaks monotonically increase with increasing LET, and begin to saturate as the device non-linearities begin to limit the response. The data show that the transient peaks produced by strikes on the *pnp* circuit are significantly lower than those produced by strikes on the *npn* circuit. In addition, the collected charge (i.e., mathematical integration of the output current as a function of time for a 50 Ω load) for both circuits monotonically increase with increasing energy, with the collected charge from the *npn* circuit increasing at a faster rate.

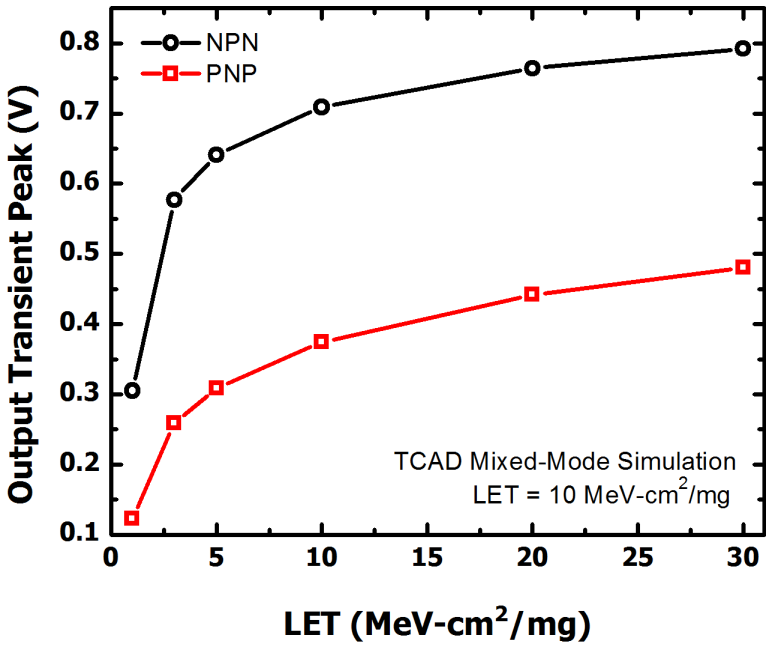


Figure 29: Transient peaks as a function of linear energy transfer when a heavy ion passes through the common-emitter device of the *npn* and *pnp* LNAs.

3.5 Discussion

The presented results show that, in the context of RF circuits, *pnp* devices still show increased robustness to single-event transients by exhibiting lower transient peaks and collected charge across all simulated LETs. However, the performance for the circuit designed with *pnp* devices is also lower. This was not the case for the comparator pre-amplifiers because, being analog circuits, their frequency of operation was too low to show major discrepancies in performance. However, at these higher

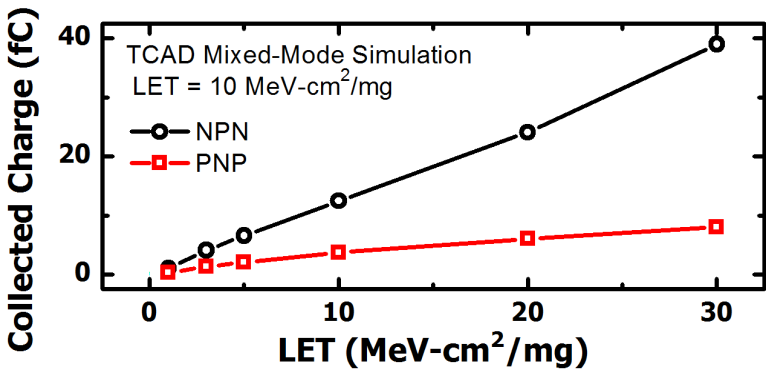


Figure 30: Collected charge as a function of linear energy transfer when a heavy ion passes through the common-emitter device of the *npn* and *pnp* LNAs.

frequencies, the LNA resulting from using only *pnp* devices has lower gain, higher noise figure, and lower P1dB. A natural question results: is the added robustness to heavy-ion phenomena worth the decrease in circuit performance? The answer to this question depends on several factors, including radiation environment, type of received data, required receiver performance, etc. Therefore, it is difficult do answer without making assumptions about the intended application. Although the *pnp* LNA has less performance than the *npn* LNA, it also consumes less *dc* power. Power consumption could be traded-off for increased gain with marginal increases in NF, which could make the *pnp* design viable. Ultimately, the choice would depend on the system specifications.

3.6 Summary

We have shown through simulation that the single-event transient response of LNAs designed with *pnp* devices exhibit lower transient peaks and collected charge when compared to an LNA designed with *npn* devices. However, we have also shown through simulation that, by using the same design procedure, the *pnp* LNA also has less performance than the *npn* LNA. The impact of the trade-off between circuit performance and SET robustness will be application-specific and it is difficult to choose one over the other without making assumptions about the desired application.

However, the performance of the *pnp* circuit could be improved using circuit design techniques, which could potentially be enough for a given application. Therefore, *pnp* devices should not be ruled out as a mitigation strategy for RF circuits.

At the time of this writing, these designs have been submitted for fabrication and will be measured once the hardware returns from the foundry.

CHAPTER IV

SINGLE-EVENT UPSET MITIGATION IN A COMPLEMENTARY SIGE HBT BICMOS PLATFORM

4.1 Introduction

The work presented in the previous chapters showed that bulk complementary platforms could be used to enable radiation tolerant circuits due to the reduced SEE sensitivity of *pnp* devices. However, the data presented in these chapters were from pulsed-laser testing and TCAD simulation. Although SETs produced from pulsed-laser testing are representative of those resulting from heavy ions, and serves as a comparative aid between multiple circuits, it is difficult to relate these results to the circuit sensitivity in space-based environments. Furthermore, it is difficult to quantify the effects of analog transients at the system level. Shorter transient peaks and duration may not necessarily translate to data corruption. Therefore, this chapter presents the study of the single-event upset (SEU) response of high-speed digital test structures measured using a heavy-ion broad beam. Utilizing a digital test structure allows for the use of bit-error-rate (BER) as a metric for comparison between both circuits.

4.2 Experimental Details

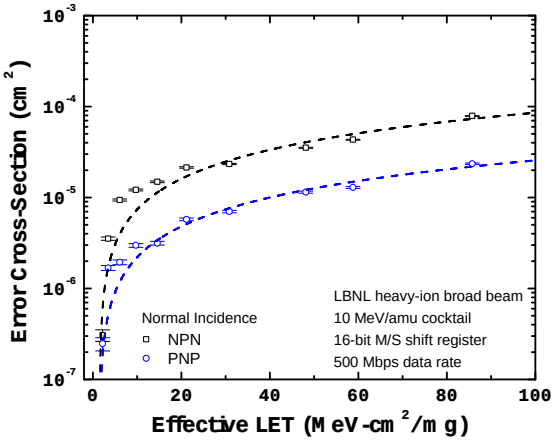
16-bit digital shift registers with an master/slave architecture were designed using the IHP SG25H3P SiGe BiCMOS process. Both shift registers were designed for a 300 mV input and output swing, and incorporated an RHBD gated-feedback cell (GFC) clock tree to decouple clock-derived multiple bit upsets (MBUs) from the overall circuit-level SEU response [35]. In each design, only *npn* or *pnp* devices were utilized for all

D-flip-flops (DFFs), clock tree buffers, and data buffers. The drawn dimensions and device-to-device spacing were matched to minimize differences in the designs. The shift registers were die-attached, wirebonded onto custom-designed high-frequency test boards, and taken to Lawrence Berkeley National Laboratorys BASE facility for SEE characterization, using the 10 MeV/amu heavy-ion cocktail across multiple linear energy transfers (LETs) and data rates (500 Mbps, 1 Gbps, 3G bps). All test packages were monitored in-beam with an Anritsu MP1764 BERT analyzer, utilizing a 127-bit pseudo-random pattern generator and error detector. The current densities within each shift register were selected to provide the fastest switching speeds (i.e., current density near peak f_{T}). All comparisons are made at a normal incidence angle, unless otherwise noted.

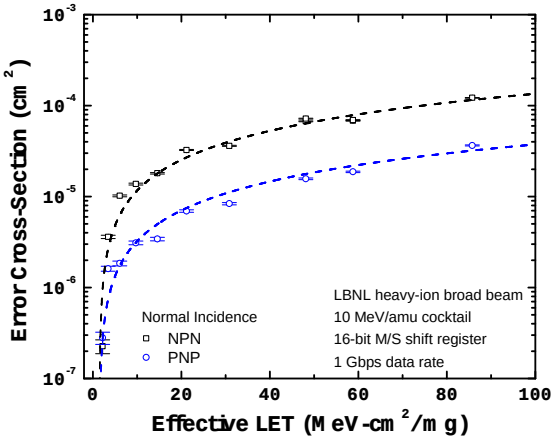
4.3 Heavy-Ion Broad-Beam Results

The measured BER cross-sections for both 16-bit shift registers across multiple data rates are shown in Fig. 31. Both digital structures exhibit an increase in bit errors as a function of LET, as expected. In addition, the BER cross-sections also increase with increasing data rates. This is also expected since, for a given heavy-ion strike duration, more bits will be shifted in this time, and therefore a higher number of bits can be flipped. However, the *pnp* shift register shows significant reductions in its ion-induced SEE response across all LETs and data rates when compared to the *npn* shift register. At a data rate of 500 Mbps, the *pnp* shift register shows a 3.3X reduction in the error cross-section, while at 1 Gbps and 3 Gbps it shows a 3.8X and 4.3X reduction, respectively. Therefore, the SEU/MBU improvement provided by *pnp* SiGe HBTs appears to increase at higher clock frequencies and data rates. To gain a better understanding on the internal transient dynamics occurring within these high-speed digital test structures, a plot of the difference between bit errors and error intervals is shown in Fig. 32 and a plot of the ratio of multiple bit errors (i.e.,

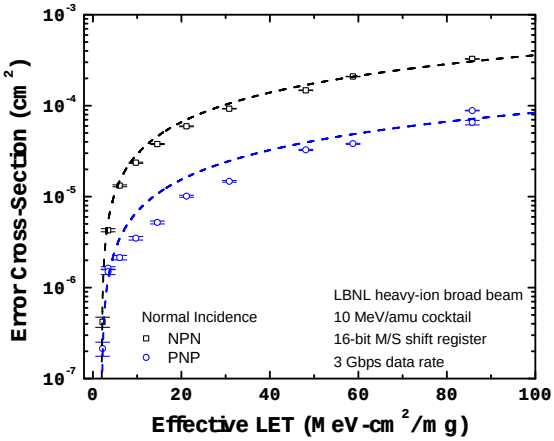
clock errors and MBUs) to the total number of bit errors is shown in Fig. 33.



(a) 500 Mbps Data Rate



(b) 1 Gbps Data Rate



(c) 3 Gbps Data Rate

Figure 31: Measured bit-error cross-sections for the npn and pnp 16-bit master/slave shift registers as a function of LET at three different data rates (500 Mbps, 1 Gbps, 3 Gbps). All measured data are at a normal ion incidence angle.

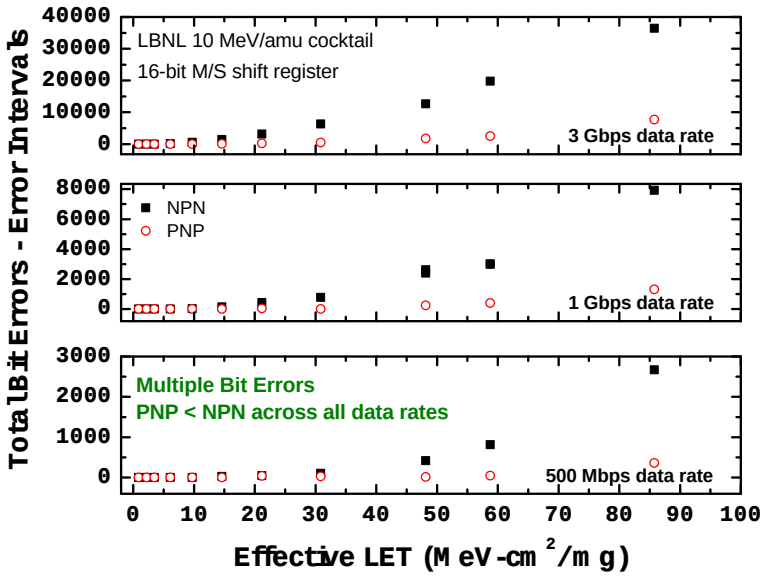


Figure 32: Difference in total bit errors and the number of bit-error intervals (time interval = 1 ms) measured by the Anritsu MP1764 BERT as a function of LET for npn and pnp shift registers across multiple data rates.

Error intervals, a dimensionless quantity calculated internally by the Anritsu BERT analyzer, increments if an error event occurs outside of a pre-defined time interval (1 ms for the entire heavy-ion experiment). If multiple errors occur within this time interval, the BERT analyzer still registers the events as a single error interval; therefore a greater number of error intervals indicate that SEUs compose a majority of the total bit errors. As shown in Fig. 32, the *pnp* shift register exhibits a minor increase in multiple bit errors (i.e., clock errors and/or MBUs), which is expected since the faster clock rate has a greater probability of shifting multiple bits during a heavy-ion strike. However, the *npn* shift register exhibits significantly more multiple bit errors, especially at higher ion-strike LETs. Similarly, the *pnp* designs exhibit a lower fraction of multiple bit errors across all three data rates, as shown in Fig. 33. Since all of these BER measurements were taken at a normal ion incidence, the large increase in multiple bit errors may indicate that the npn clock/data buffers and DFFs are highly sensitive to charge sharing between the collector and bulk silicon substrate, particularly for higher-LET ion strikes which deposit more energy into the

surrounding silicon lattice. Since the transistor-to-transistor spacing for both designs was minimized down to the SG25H3P process design rule limits (i.e., a worst-case analysis), these high charge concentrations near the device volumes may be the cause of the elevated cross-sections for the *npn* shift register. It should be noted that the IHP SG25H3P platform does not include deep trench isolation, making charge sharing easier between devices. The enhanced isolation between the output (collector) terminal and substrate due to the n-well isolation layer in the *pnp* device, as previously reported in [27], could be driving the observed reductions in error cross-section.

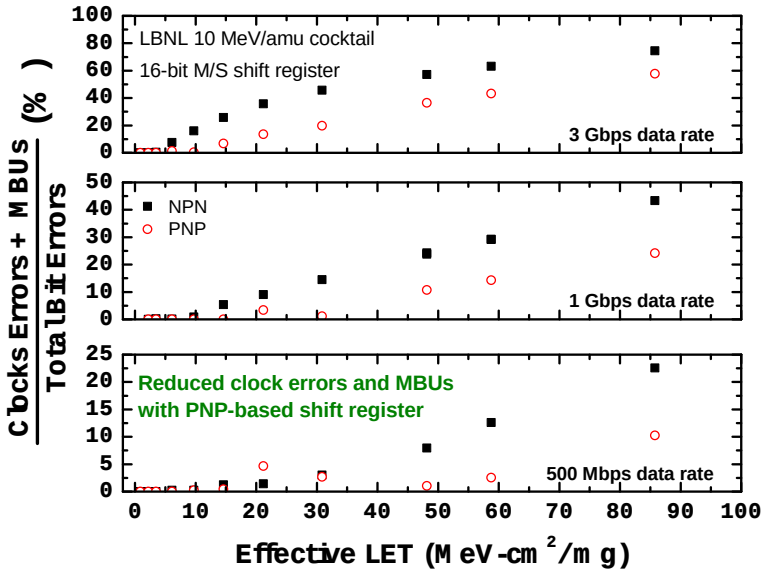


Figure 33: Ratio of multiple bit errors (clock errors and MBUs) to the total number of bit errors measured by the Anritsu MP1764 BERT as a function of LET for npn and pnp shift registers across multiple data rates.

4.4 Summary

We presented heavy-ion broad-beam SEE results for digital test structures designed in a third-generation complementary BiCMOS process. High-speed digital shift registers designed using only *pnp* SiGe HBTs exhibit a large reduction (approximately one order of magnitude) in bit-error-rate (BER) cross-section when compared to a shift

register designed using only *npn* devices. The possible driving force behind this decrease in BER cross-section could be the n-well isolation required to fabricate the *pnp* device in a complementary process. This layer would prevent charge induced by a heavy-ion from being collected by the output nodes (i.e., collector terminals). However, more experiments, designed specifically for charge sharing measurements, need to be performed to confirm this hypothesis.

CHAPTER V

CONCLUSION

This work has evaluated a complementary silicon-germanium platform for extreme environment applications, specifically high-radiation environments. Circuits in the analog, digital and RF domain have been designed for radiation testing and their radiation response has been studies using pulsed laser measurements, heavy-ion measurements and TCAD simulations. All of the presented circuits show that the circuits designed using *pnp* devices enjoy an improved radiation response when compared to identically designed *npn* circuits. The heavy-ion data presented, validate results from TCAD simulations and pulsed-laser experiments and show an increased robustness of *pnp* devices to heavy-ion induced transient phenomena. Therefore, it would be of interest to designers to consider the use of *pnp* devices in circuits and systems for radiation-intense applications. In addition, using *pnp* devices could enable new forms of radiation-hardening-by-design techniques by using new circuit topologies that take advantage of these devices.

5.1 Contributions

Chapter 2 presented the first circuit-level study of the single-event transient in a bulk, complementary SiGe BiCMOS platform, The results from this work were presented at the 2016 IEEE Nuclear and Space Radiation Effects Conference (NSREC) and were published in the IEEE Tansactions of Nuclear Science [3].

Chapter 3 focused on comparing the trade-offs between RF performance and single-event transient response of low-noise amplifiers designed using only *npn* and only*pnp* devices. The work presented in this chapter will be submitted for publication to the IEEE transactions of Nuclear Science after these circuits have been measured.

Chapter 4 presented the first heavy-ion measurements in a bulk, complementary SiGe BiCMOS platform using digital test structures. The results from this work have been accepted for presentation at the 2017 IEEE Nuclear and Space Radiation Effects Conference (NSREC) and are slated for publication in the IEEE Transactions of Nuclear Science.

5.2 Future Work

Although substantial work has been done to assess the performance of C-SiGe platforms for radiation environments in the analog, digital and RF domains, there are several aspects that need to be explored. The following list presents several ideas to extend this research:

1. Measure the single-event response of the simulated *npn* and *pnp* low-noise amplifiers using a radiation source such as heavy-ion beam or two-photon absorption laser.

2. Design, implement and measure circuits that use both *npn* and *pnp* devices as a radiation-hardening-by-design approach.

3. Characterize the designed low-noise amplifiers at low temperatures to determine changes in performance as a function of temperature.

4. Perform cryogenic *ac* measurements such as f_{T}, f_{MAX}, linearity, and source- and load-pull measurements on *npn* and *pnp* devices to explore changes in *ac* performance across temperature.

5. Utilize *npn* and *pnp* over-temperature data to develop circuits optimized for cryogenic operation.

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